COM-HPC-Mini

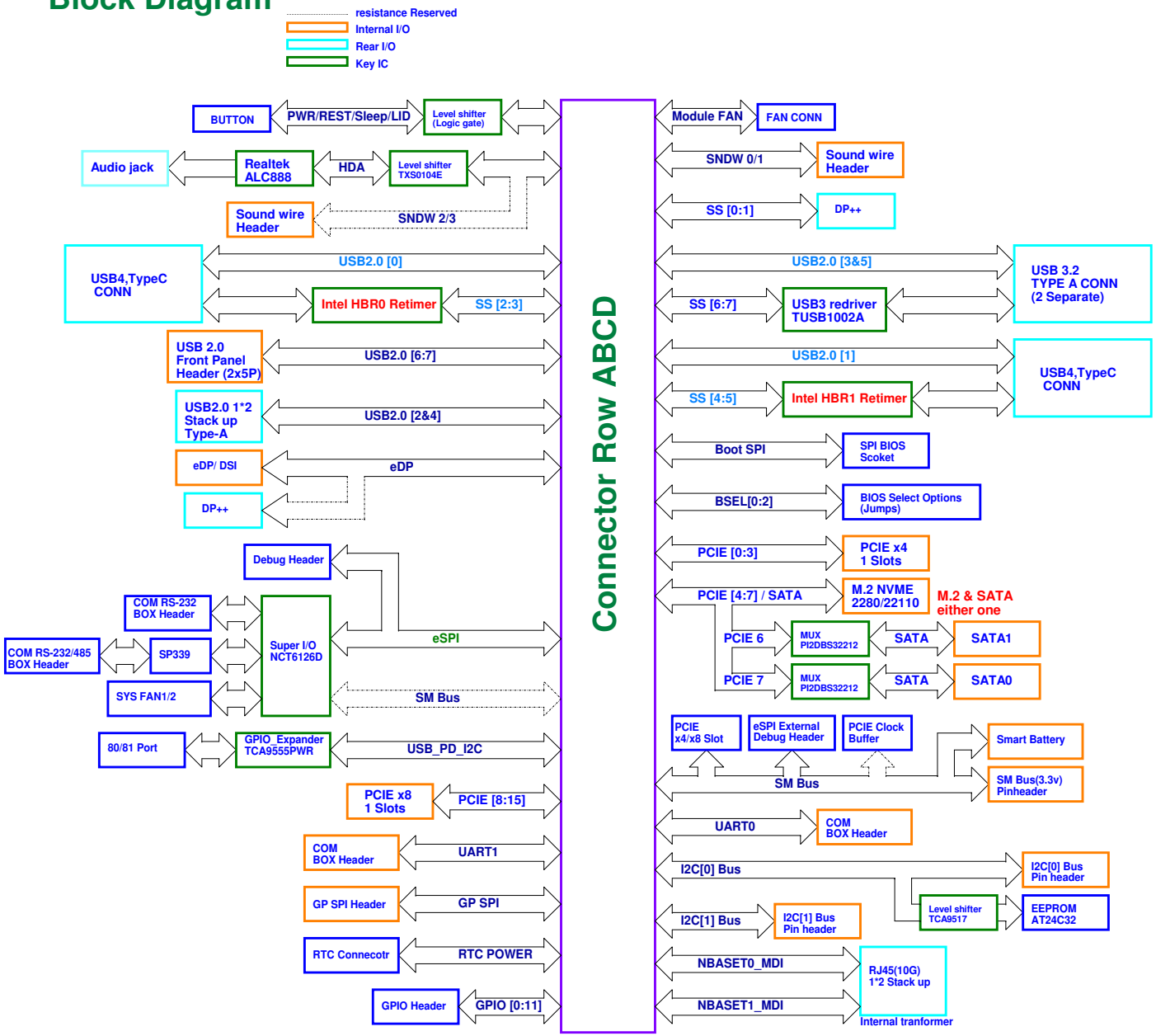
COM-HPC-Mini Base
PICMG COM-HPC CDG Rev 2.2
PICMG COM-HPC MBS Rev 1.2 Draft V0.51c

Rev.A1

PCB Size : 304.8 mm x 243.84 mm
(12000 mils x 9600 mils)

ADLINK P/N : 51-77110-0A10

Block Diagram



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Title: Cover Page & Block Diagram

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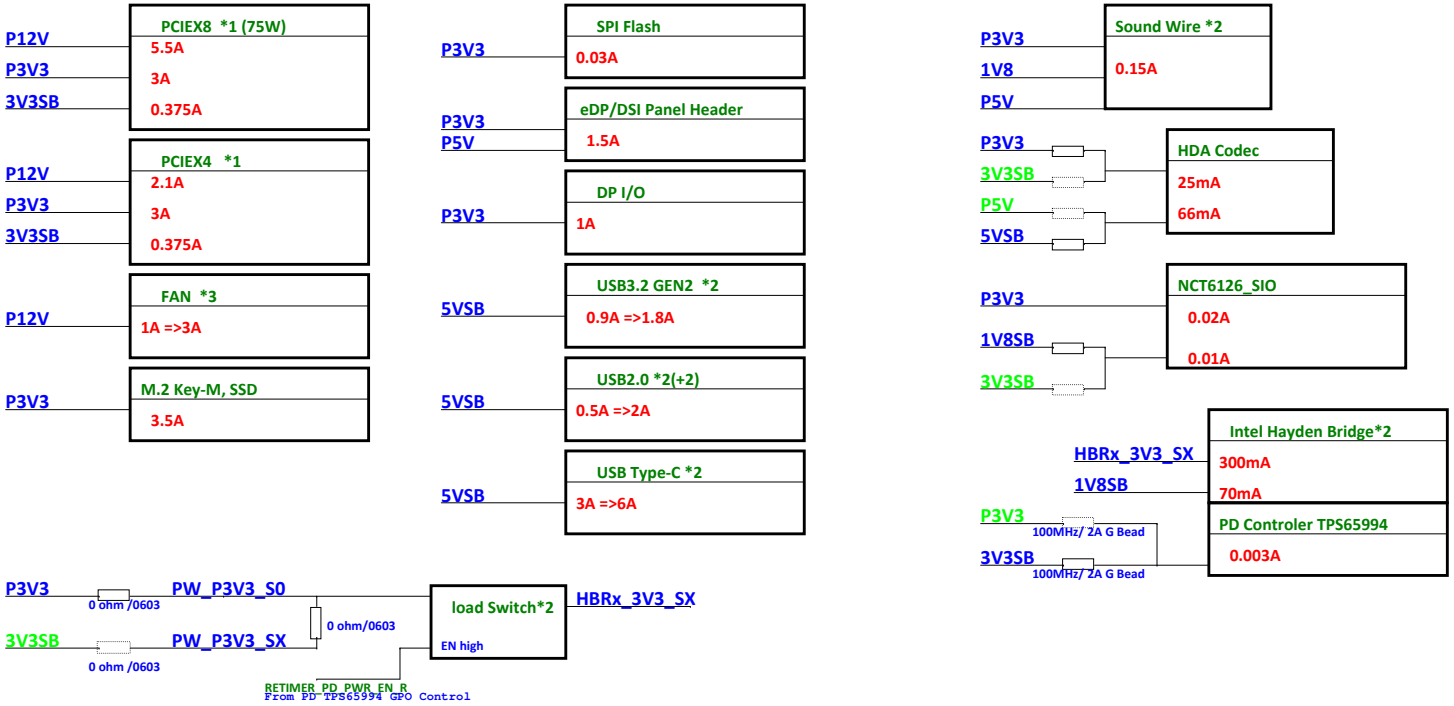

P12V ===> 10.6A
5VSB ===> 9.9A (with P5V)
3V3SB ===> 1.2A (with 1V8SB)
1V8SB ===> 0.08A
P3V3 ===> 13.2A (with 1V8)
1V8 ===> 0.15A

Table 123: Input Power – Wide Range Vin – Mini Module

Power Rail	Module VCC Pin Current Capability 20% derated (Amps)	Input Range (Volts)	Minimum Input (Volts)	Max Module Input Power (at minimum input voltage) (Watts)	Assumed Conversion Efficiency	Max Module Load Power at minimum input voltage (Watts)
VCC	12 * 1.12 = 13.4	8 - 20	8.0	107	85%	91
VCC_RTC	1.12	2.3 - 3.3	2.3			

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Title: Power Distribution

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resistance Reserved

SMBUS/ I2C

Connector Row ABCD

SMBus
C86/C87

PICMG 3.0: Standby power

Level shifht Buffer TCA9517A

P_+1V8SB to 3V3SB

N-MOS

2.2k

P3V3

PCIE Clock Buffer RC19004A — Address: D8h

Super I/O NCT6126D — Address: 2Eh

PCIE x4 Slot

PCIE x8 Slot

eSPI External Debug Header

Smart Battery

Level shifht Buffer TCA9517A

SM Bus(3V3SB) Pinheader

PICMG 1.0: S0 power
PICMG 2.0: Standby power
PICMG 3.0: Standby power

I2C0 Bus
C93/C94

Level shifht Buffer TCA9517A

P_+1V8SB to 3V3SB

EEPROM AT24C02D — Address: A4h

Smart Battery

Level shifht Buffer TCA9517A

I2C0 Bus(3V3SB) Pin header

I2C1 Bus
C96/C97

Level shifht Buffer TCA9517A

I2C1 Bus(P_+1V8SB) Pin header

Standby power
USB4_PD_I2C
B35/B36

N-MOS

P_+1V8SB to 3V3SB

I/O Expander TCA9555PWR — Address: 4Eh

SML1
B29/B30
(1MHz)
Standby power

N-MOS

P_+1V8SB to 3V3SB

PD Controler TPS65994BH — I2C

PD I2C, 7 bits
Port A: 20h, Port B: 24h

SML1 slave
TBC

SML0
B32/B33

Hayden Bridge JHL9040R — I2C TBC

Hayden Bridge JHL9040R — I2C TBC

499ohm supports 1MHz speed (Default)
2.2Kohm supports 400MHz speed.
10Kohm supports 100KHz speed.

CLK

Connector Row ABCD

PCIe_REFCLK0_LO
PCIE Lane [0:7]
C59/C60

PCIe_REFCLK0IN
A11/A12

PCIe_REFCLK0_HI
PCIE Lane [8:15]
C56/C57

PCIE Clock 1to 4 Buffer RC19004AGNL

85 ohm
100 MHz

DIF0 — PCIE x 4 SLOT

DIF1 — M.2 M Key

PCIE x 8 SLOT

eSPI_CLK
A54

15 ohm

0 ohm — CLK1 — Super I/O NCT6126D

0 ohm — CLK2 — eSPIExternal Debug Header

19.2MHz-33 MHz

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Title: SMBUS/I2C/CLK Distribution

Size: A3 | Document Number: COM-HPC Mini Base | Rev: A1

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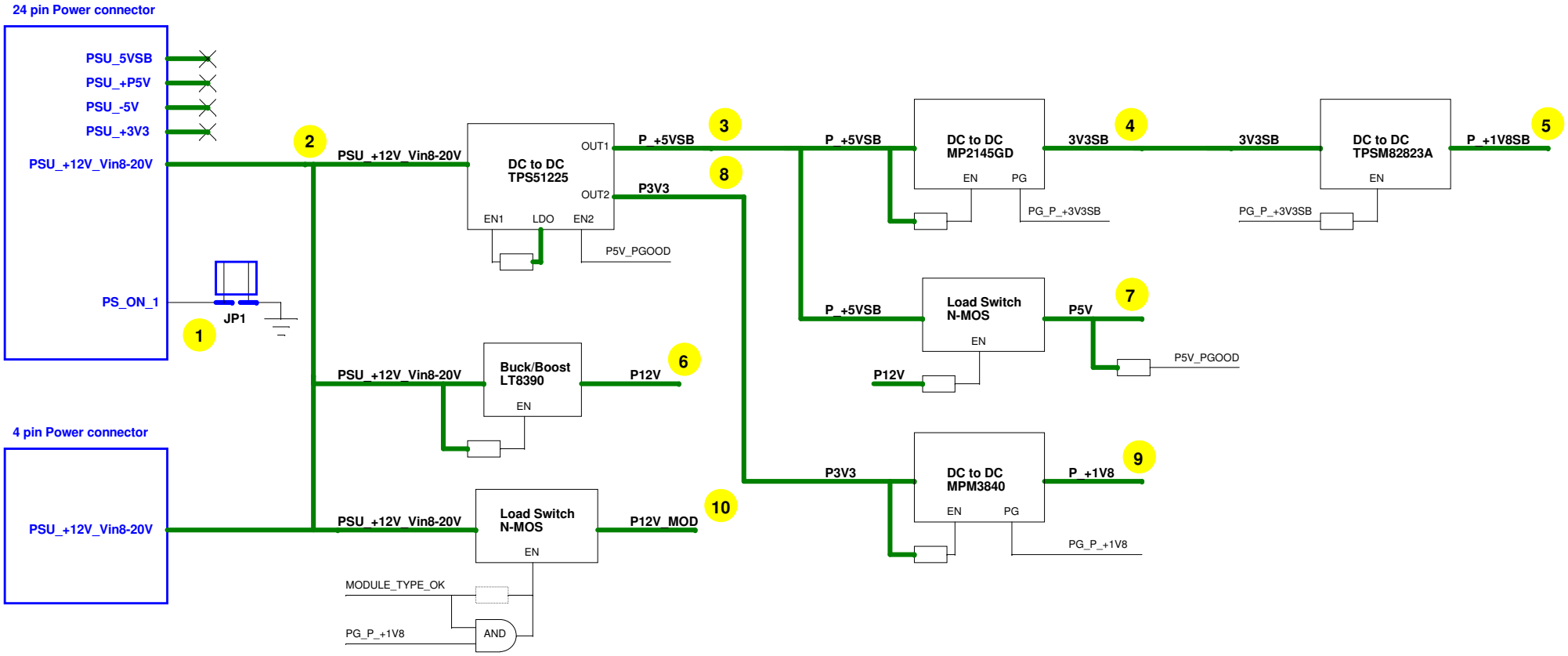

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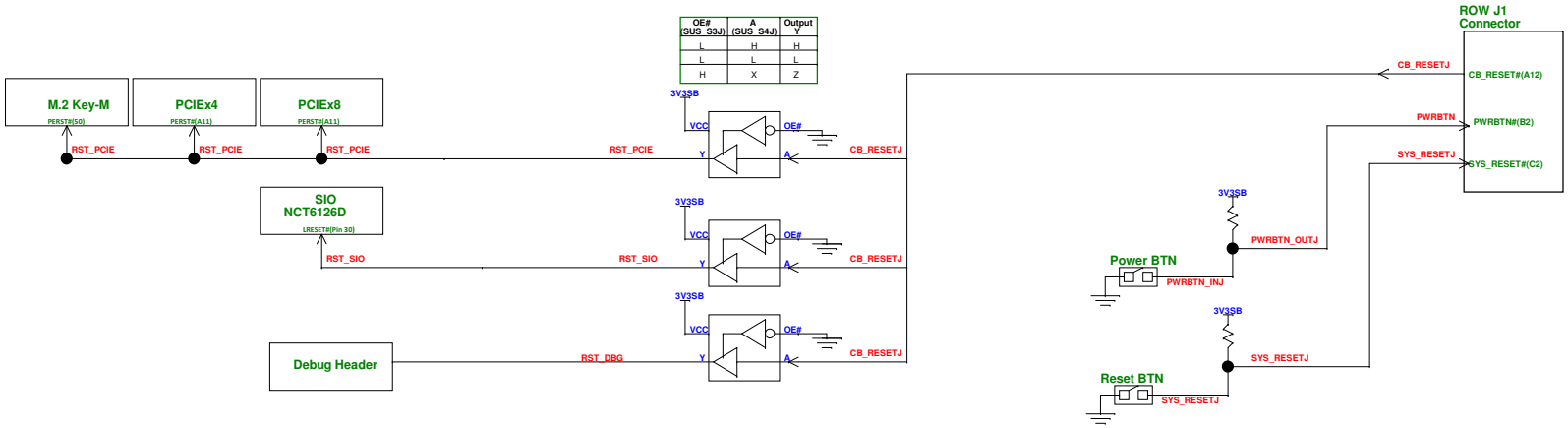
Title: Power Delivery

Size: C | Document Number: COM-HPC Mini Base | Rev: A1

Date: Wednesday, May 21, 2025 | Sheet 4 of 43



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Title: Reset

Size	Document Number	Rev
A	COM-HPC Mini Base	x1

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Title

Reserved

Size	Document Number	Rev
C	COM-HPC Mini Base	A1

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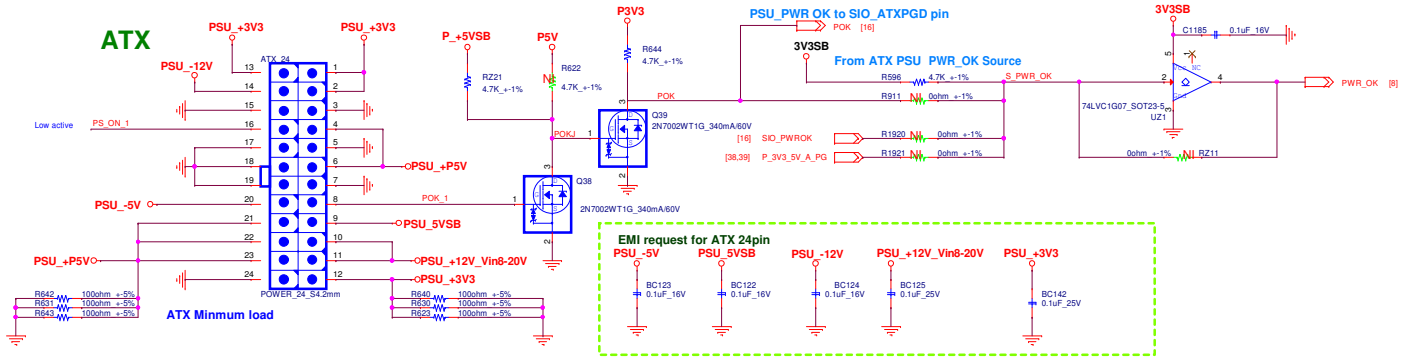
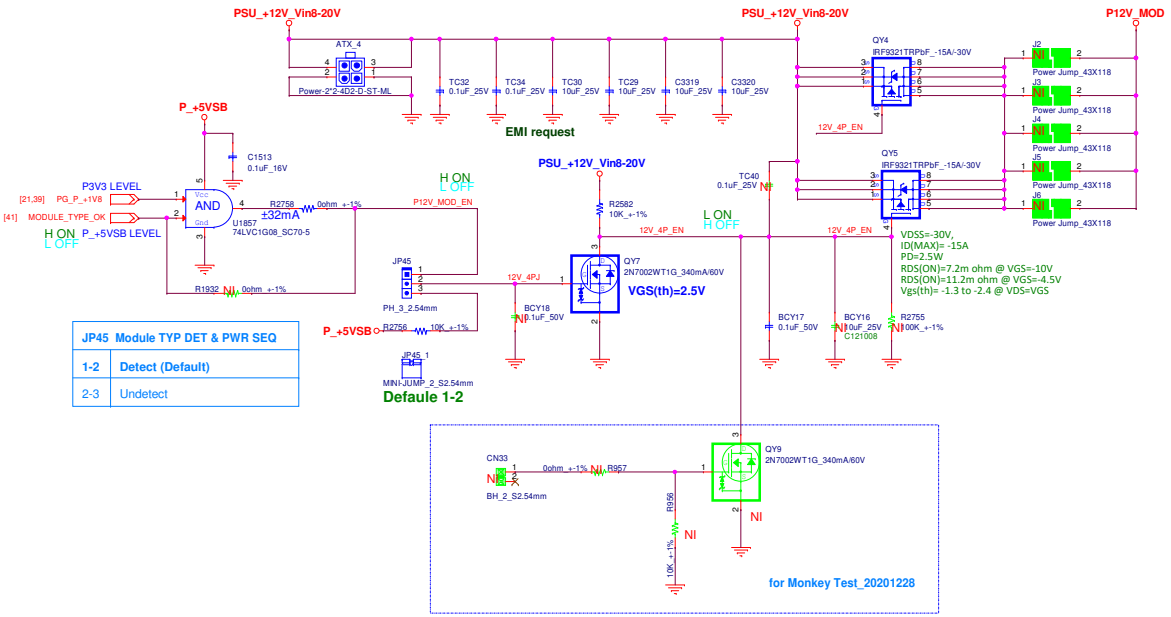


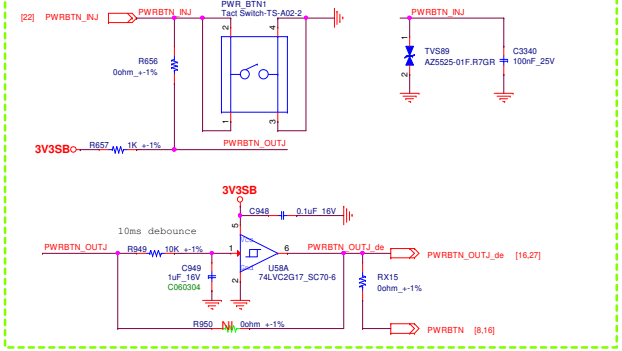
Power strategies	JP1
AT mode (ATX PSU)	3-4
AT mode (Smart Battery)	1-2

Module Main Power (P-MOS)

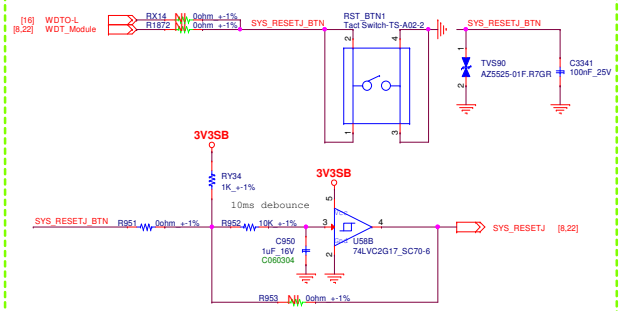


JP45 Module TYP DET & PWR SEQ	
1-2	Detect (Default)
2-3	Undetect

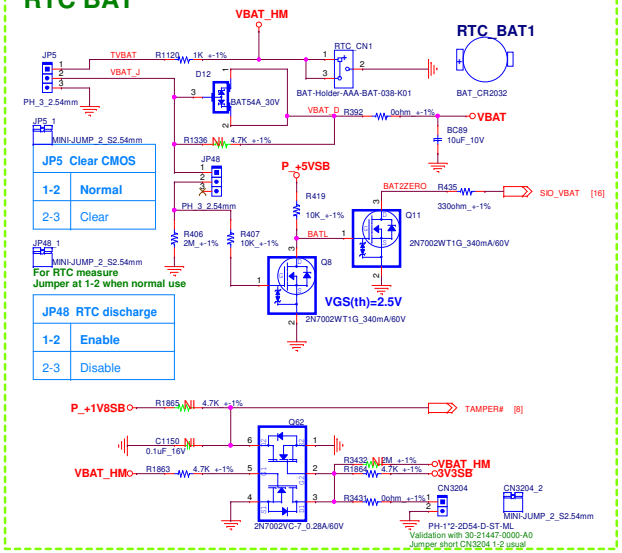
PWR BTN



RST BTN



RTC BAT



JP5 Clear CMOS	
1-2	Normal
2-3	Clear

For RTC measure
Jumper at 1-2 when normal use

JP48 RTC discharge	
1-2	Enable
2-3	Disable

Validation with 30-21447-0000-A0
Jumper short CN3204 1-2 usual

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Title: ATX24_Power&PWR_SYS REST_BTN
Size: Custom
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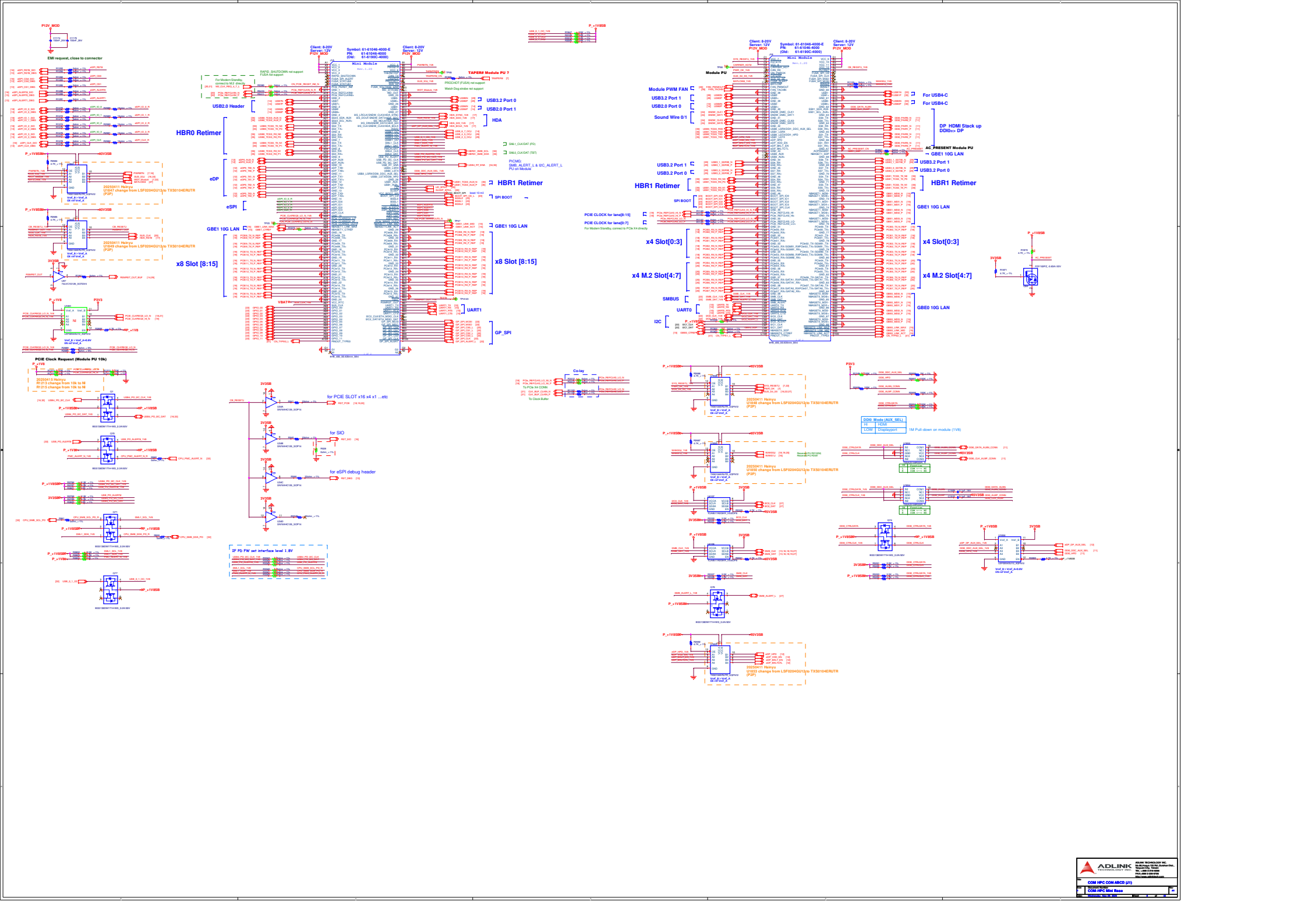
P12V_MOD
EMI request, close to connector
HBR0 Retimer
eDP
eSPI
x8 Slot [8:15]
USB2.0 Header
GBE1 10G LAN
Mini Module
Symbol: 61-61046-4000-E
P/N: 61-61046-4000
(Old: 61-6190C-4000)
Client: 8-20V
Server: 12V
P12V_MOD
USB3.2 Port 0
USB2.0 Port 1
HDA
HBR1 Retimer
SPI BOOT
GBE1 10G LAN
x8 Slot [8:15]
UART1
GP_SPI
TAPER® Module PU ?
PROCHOT (FUSA) not support
Watch Dog strobe not support
RAPID_SHUTDOWN not support
FUSA not support
For Modern Standby, connect to M.2 directly
PICMG: SMB_ALERT_L & I2C_ALERT_L PU on Module
Module PU
Module PWM FAN
USB3.2 Port 1
USB2.0 Port 0
Sound Wire 0/1
HBR1 Retimer
SPI BOOT
PCIE CLOCK for lane[8:15]
PCIE CLOCK for lane[0:7]
For Modern Standby, connect to PCIe X4 directly
x4 Slot[0:3]
x4 M.2 Slot[4:7]
SMBUS
UART0
I2C
For USB4-C
For USB4-C
DP_HDMI Stack up
DD0=> DP
AC PRESENT Module PU
GBE1 10G LAN
USB3.2 Port 1
USB3.2 Port 0
HBR1 Retimer
GBE1 10G LAN
x4 Slot[0:3]
x4 M.2 Slot[4:7]
GBE0 10G LAN
20250411 Hsinyu
U1847 change from LSF0204GU13 to TXS0104EURTR
(P2P)
20250411 Hsinyu
U1848 change from LSF0204GU13 to TXS0104EURTR
(P2P)
20250411 Hsinyu
U1846 change from LSF0204GU13 to TXS0104EURTR
(P2P)
20250411 Hsinyu
U1850 change from LSF0204GU13 to TXS0104EURTR
(P2P)
20250411 Hsinyu
U1833 change from LSF0204GU13 to TXS0104EURTR
(P2P)
20250415 Hsinyu
R1213 change from 10k to NI
R1215 change from 10k to NI
PCIE Clock Request (Module PU 10k)
for PCIE SLOT x16 x4 x1 ...etc
for SIO
for eSPI debug header
IF PD FW set interface level 1.8V
Co-lay
To Clock Buffer
To PCIe X4 CONN
DDR Mode (AUX_SEL)
HI HDMI
LOW Displayport
1M Pull-down on module (1V8)
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COM-HPC Mini Base
COM HPC COM ABCD (J1)

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Title

Reserved

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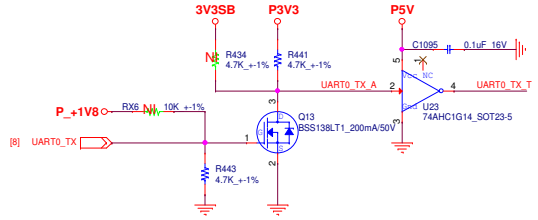
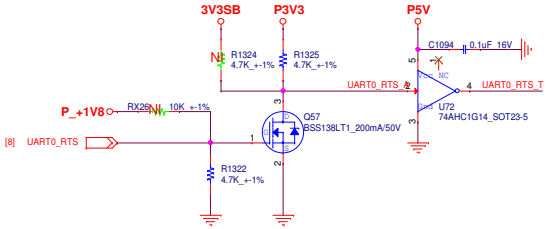
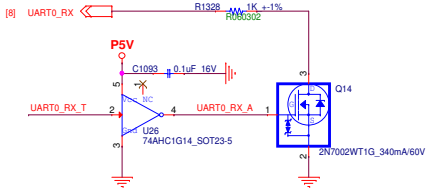
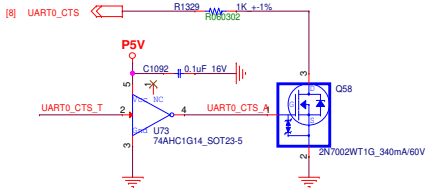
UART0 from module

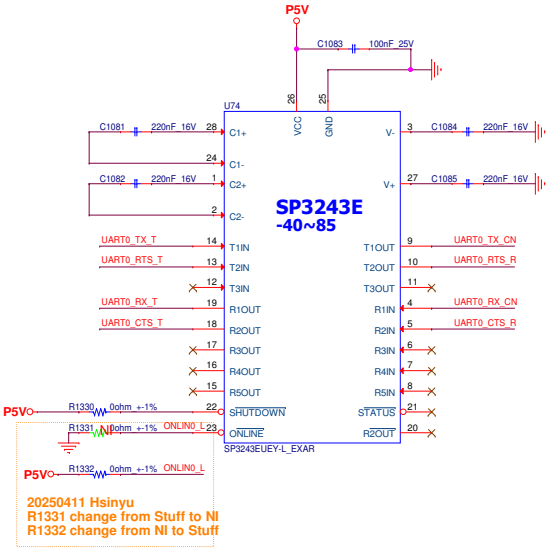
TX0 / RX0



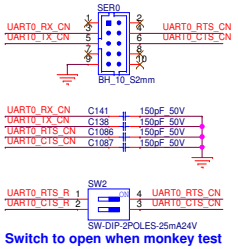






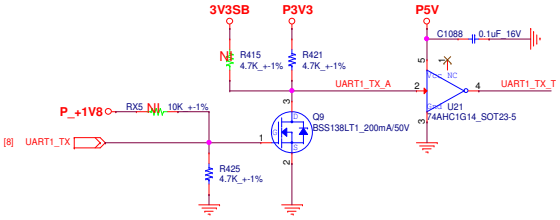


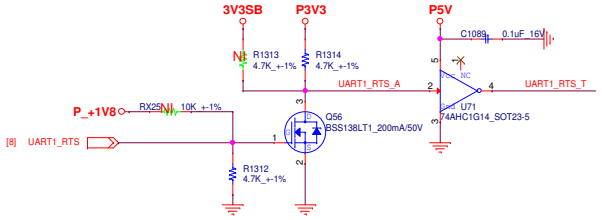
Port 0

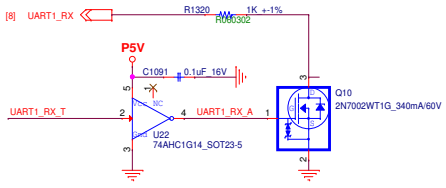


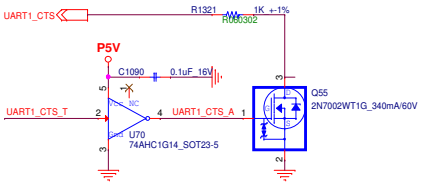
UART1 from module

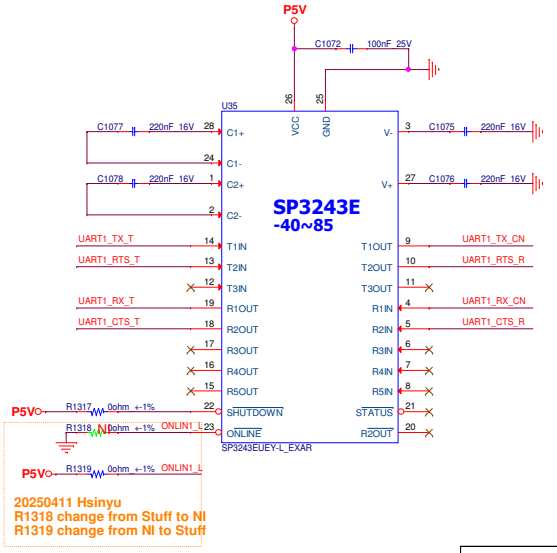
TX1 / RX1



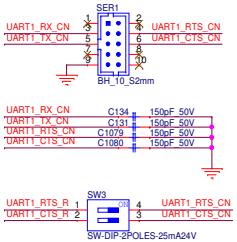








Port 1



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Title	Module series port	
Size: C	Document Number: COM-HPC Mini Base	Rev: A1
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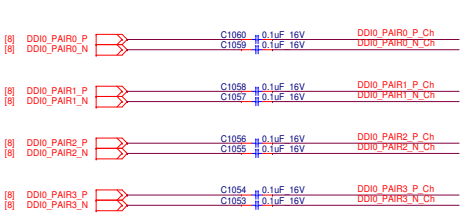
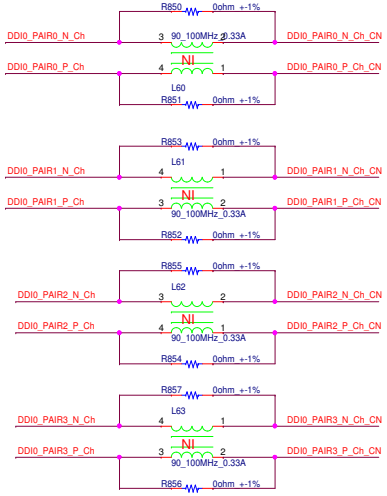
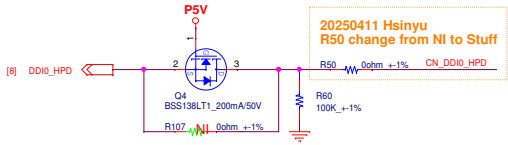
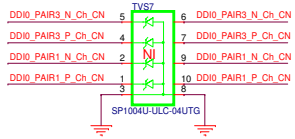
DDI0=>DP

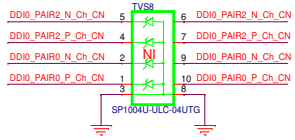
Co-layout

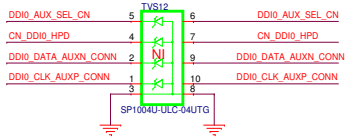


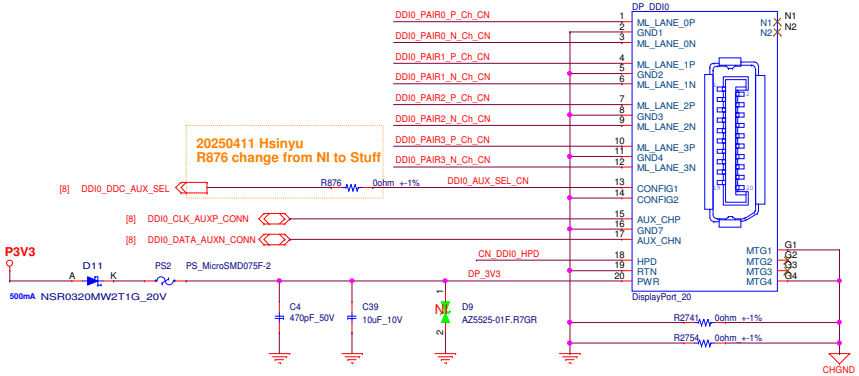












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Title	DP	
Size: C	Document Number: COM-HPC Mini Base	Rev: A1
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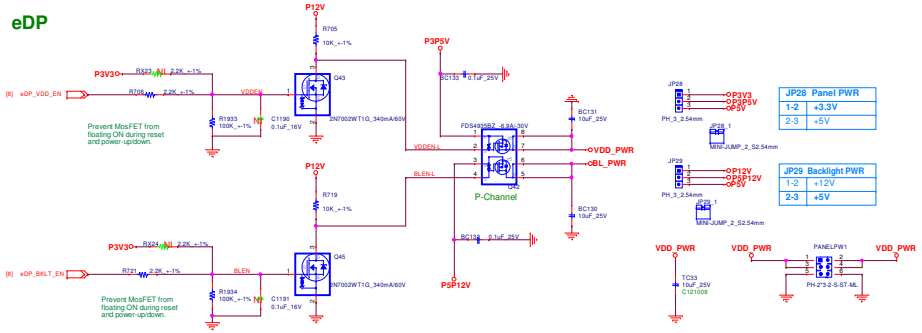
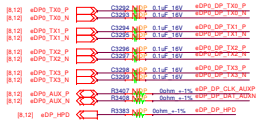
eDP



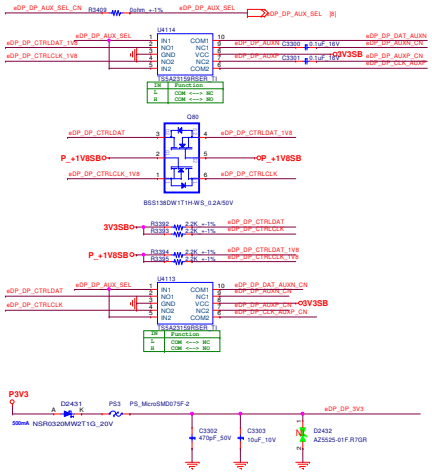
JP28 Panel PWR	
1-2	+3.3V
2-3	+5V

JP29 Backlight PWR	
1-2	+12V
2-3	+5V



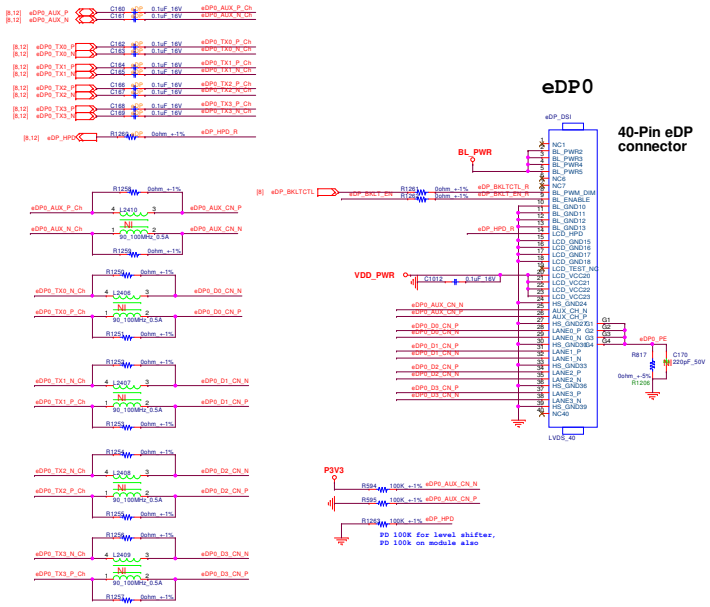
eDP_DP Mode (AUX_SEL)	
HI	HDMI
LOW	Displayport

1M Pull-down on module (1V8)

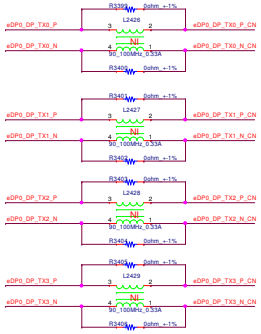


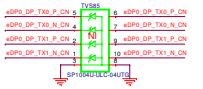
eDP0

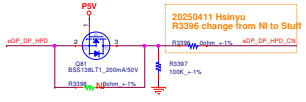
40-Pin eDP connector

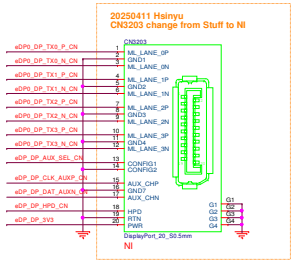


Co-layout









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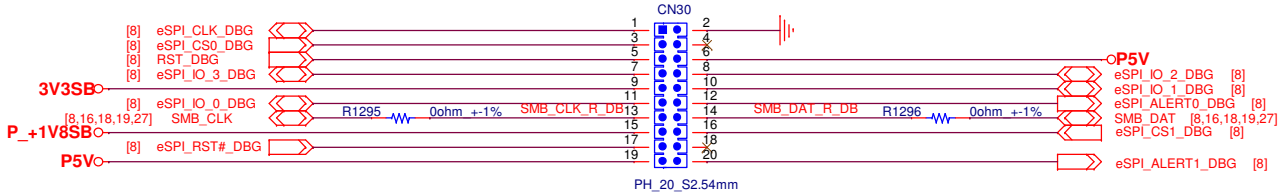
Title	eDP/DSI_Panel PWR		
Size: D	Document Number: COM-HPC Mini Base		Rev: A1
Date: Wednesday, May 21, 2025	Sheet: 12	of: 43	

Debug Header (ESPI)

Reference :

618367-TGL-H BEP Plus CRB



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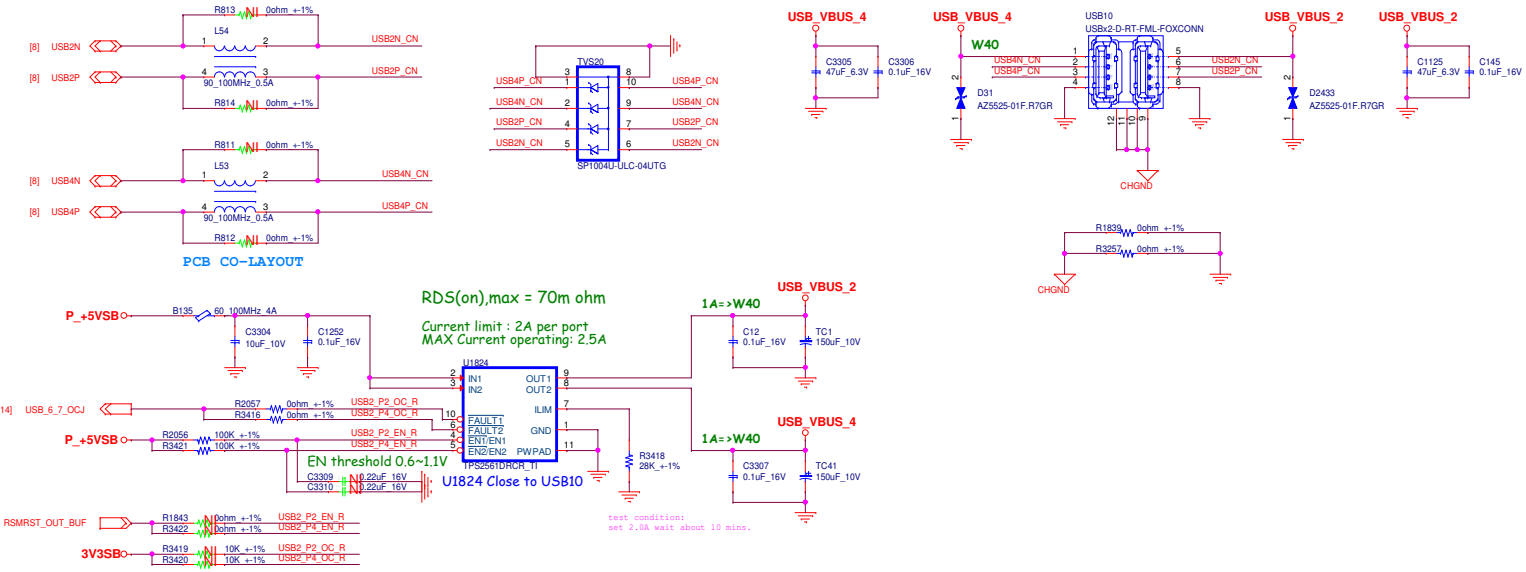
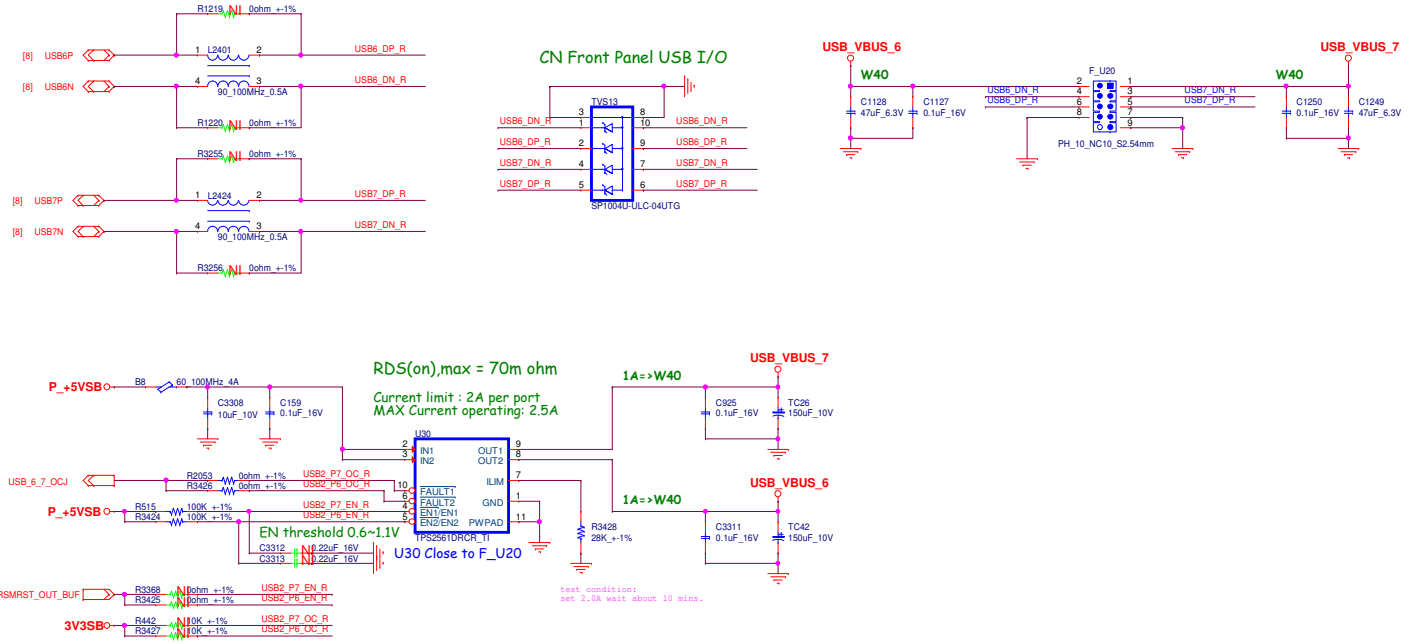
Title	eSPI DBG Header	
Size: B	Document Number: COM-HPC Mini Base	Rev: A1
Date: Wednesday, May 21, 2025	Sheet 13 of 43	

USB 2.0 [2, 4]



USB 2.0 [6:7] for Front Panel



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Title: USB 2.0 1*2 & Front USB 2.0

Size	Document Number	Rev
C	COM-HPC Mini Base	A1

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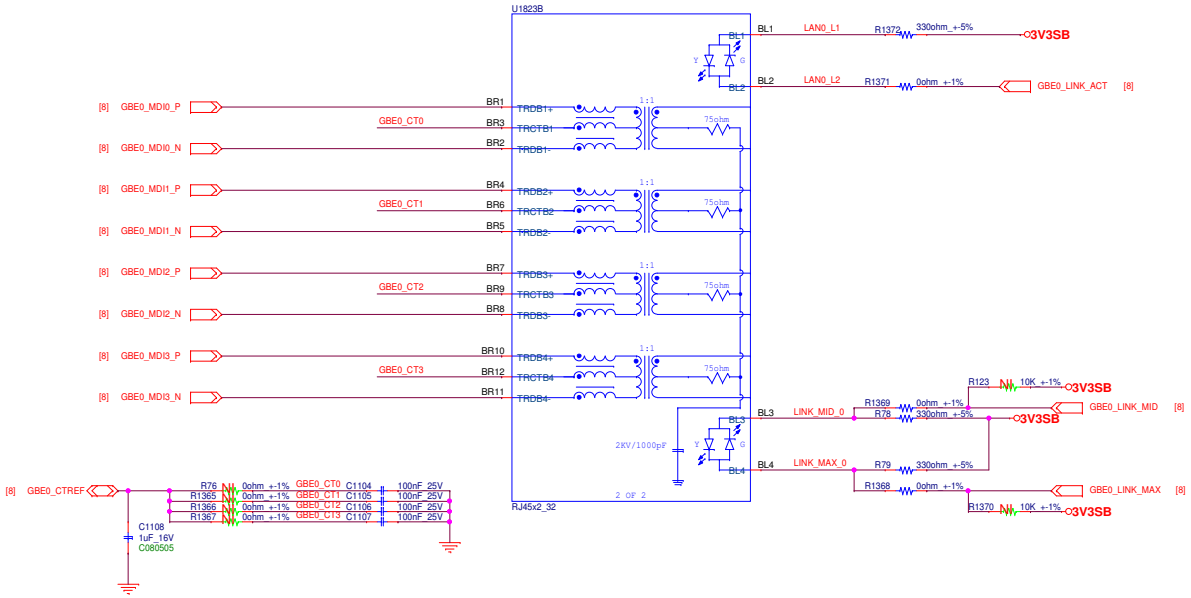
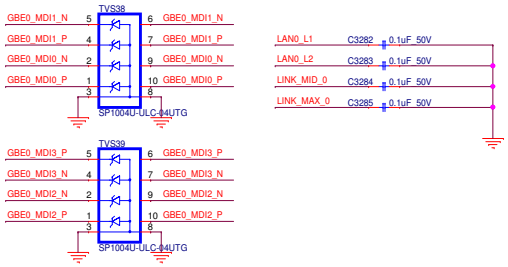
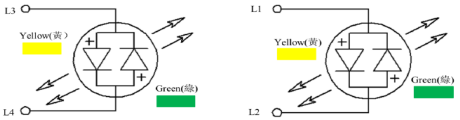
Giga LAN (10G)_RJ45 1*2 stack up

Upper Port B



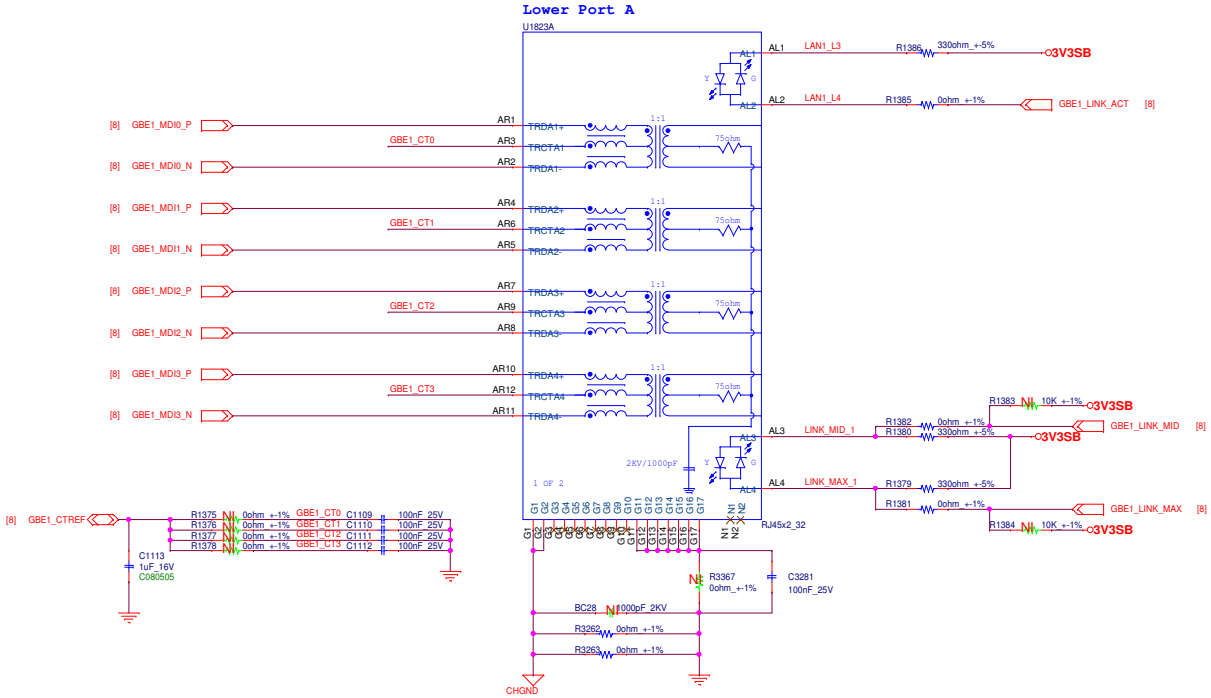
ESD Component



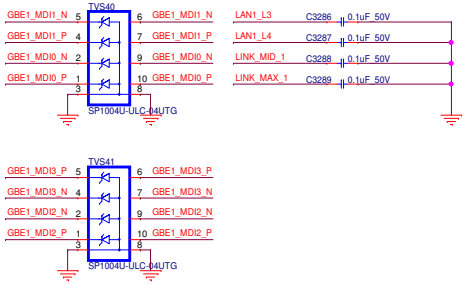


Emitting Color	λp (nm)	Vf @If=20mA	Ir @Vr=5V
Green	570	1.7 ~2.6 V	10μA max.
Yellow	588	1.7 ~2.6 V	10μA max.

Lower Port A



ESD Component



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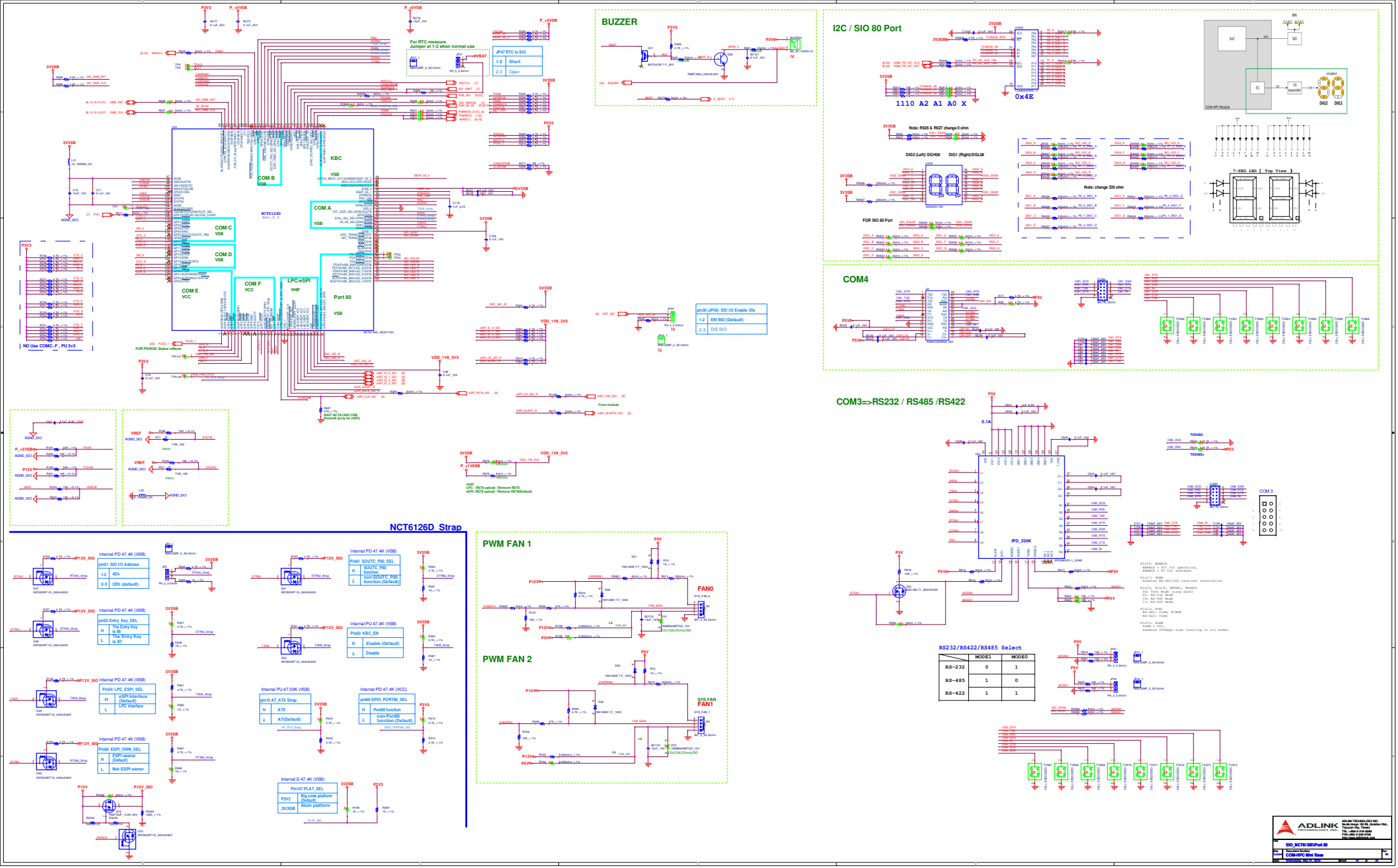
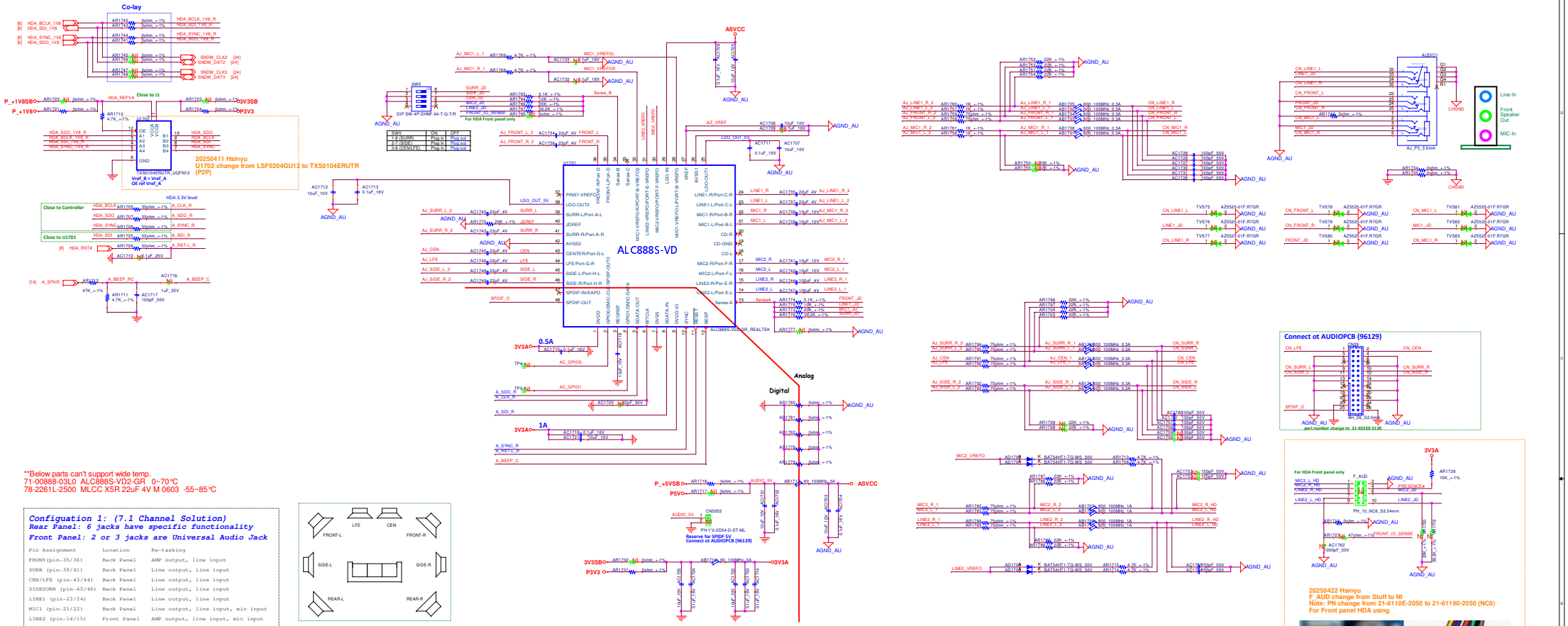
Title: Giga LAN_10G 1*2 Stack up

Size: C | Document Number: COM-HPC Mini Base | Rev: A1

Date: Wednesday, May 21, 2025 | Sheet 15 of 43


BUZZER
I2C / SIO 80 Port
COM4
COM3=>RS232 / RS485 /RS422
NCT6126D_Strap
PWM FAN 1
PWM FAN 2
KBC
COM A
COM B
COM C
COM D
COM E
COM F
LPC/eSPI
Port 80
NCT6126D
Rev_0.5
For RTC measure
Jumper at 1-2 when normal use
JP47 RTC to SIO
1-2 Short
2-3 Open
1110 A2 A1 A0 X
0x4E
Note: R626 & R627 change 0 ohm
DIG2 (Left)/ DGH0# DIG1 (Right)/DGL0#
FOR SIO 80 Port
Note: change 330 ohm
7-SEG LED (Top View)
COM-HPC Module
SoC
SIO
EC
IO expander
DIG2
DIG1
JP43 SIO I/O Enable/ Dis
1-2 EN SIO (Default)
2-3 DIS SIO
NO Use COMC-F , PU 3v3
FOR PWROK Status reflecte
From module
Internal PD 47.4K (VSB)
pin51 SIO I/O Address
1-2 4Eh
2-3 2Eh (default)
Pin61 SOUTC_P80_SEL
SOUTC_P80 function.
non-SOUTC_P80 function.(Default)
pin52 Entry_Key_SEL
The Entry Key is 88
The Entry Key is 87
Pin83 KBC_EN
Enable (Default)
Disable
Pin54 LPC_ESPI_SEL
eSPI interface (Default)
LPC interface
Pin60 ESPI_OWN_SEL
ESPI owner (Default)
Not ESPI owner
Internal PU 47.03K (VSB)
pin15 AT_ATX Strap
ATX
AT(Default)
Internal PD 47.4K (VCC)
pin69 GPIO_PORT80_SEL
Port80 function
non-Port80 function.(Default)
Internal D 47.4K (VSB)
Pin107 PLAT_SEL
P3V3 Big code platform (Default)
3V3SB Atom platform
RS232/RS422/RS485 Select
MODE1 MODE0
RS-232 0 1
RS-485 1 0
RS-422 1 1
SIO_NCT6126D#Port 80
COM-HPC Mini Base
ADLINK TECHNOLOGY INC.



**Below parts can't support wide temp.
71-00888-03L0 ALC888S-VD2-GR 0~70℃
78-2261L-2500 MLCC X5R 22uF 4V M 0603 -55~85℃

Configuation 1: (7.1 Channel Solution)
Rear Panel: 6 jacks have specific functionality
Front Panel: 2 or 3 jacks are Universal Audio Jack

Pin Assignment	Location	Re-tasking
FRONT(pin-35/36)	Back Panel	AMP output, line input
SURR (pin-39/41)	Back Panel	Line output, line input
CEN/LFE (pin-43/44)	Back Panel	Line output, line input
SIDESURR (pin-45/46)	Back Panel	Line output, line input
LINE1 (pin-23/24)	Back Panel	Line output, line input
MIC1 (pin-21/22)	Back Panel	Line output, line input, mic input
LINE2 (pin-14/15)	Front Panel	AMP output, line input, mic input
MIC2 (pin-16/17)	Front Panel	AMP output, line input, mic input

Title	HDA codec ALC888	
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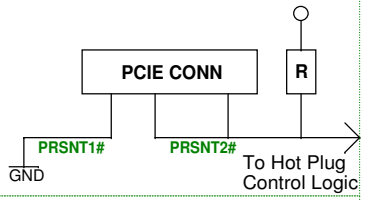
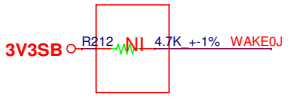
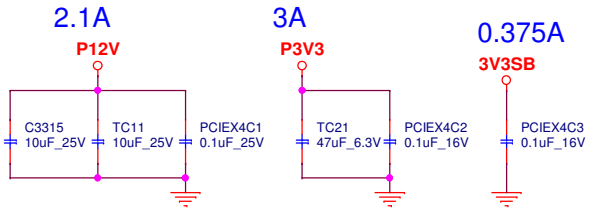
PCIe x4 Slot (PCIe 0-3)

PCI Express Hot-Plug controller detects

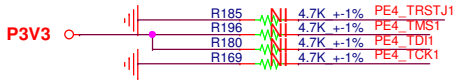


The WAKE# signal is an open drain, active low signal that is driven low by a PCI Express component to reactivate the PCI Express slot's main power rails and reference clocks.

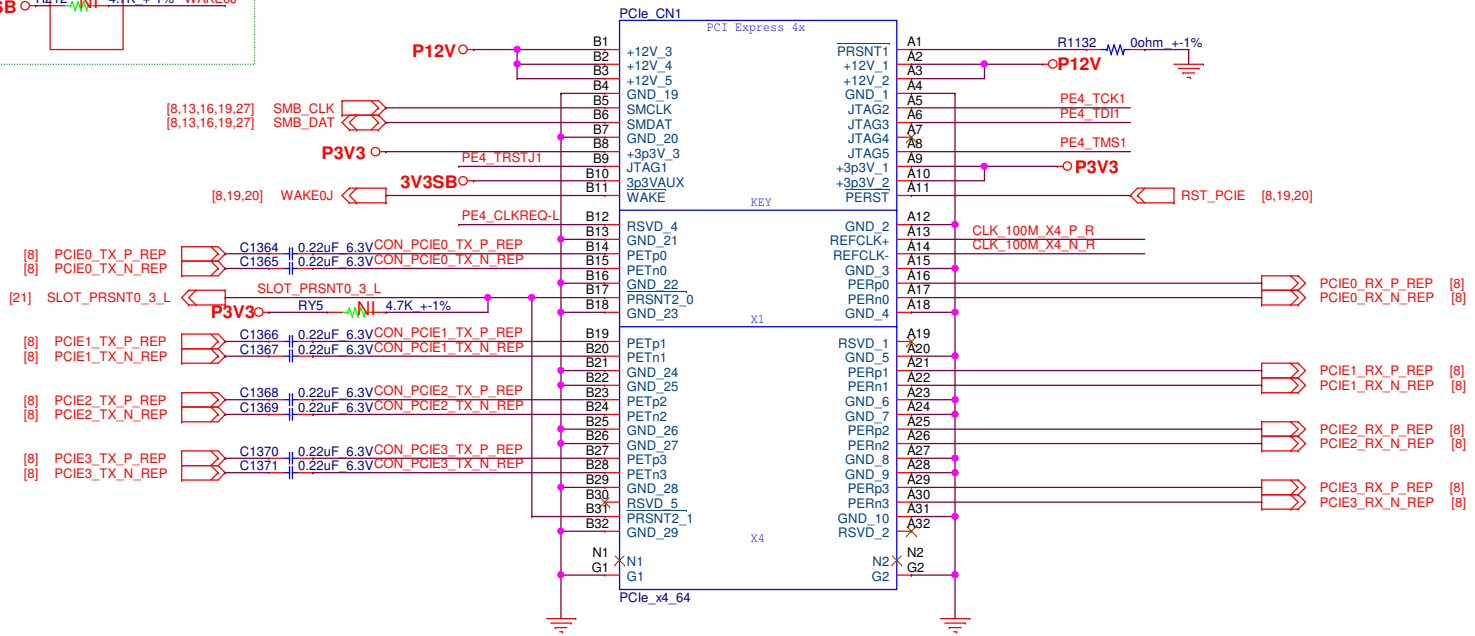




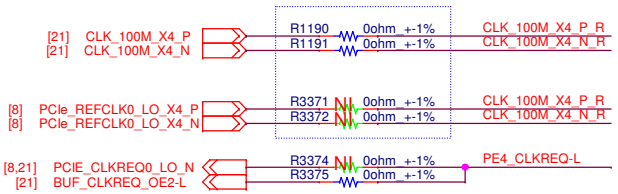
EMI request : 0.1u Cap



TX CAP close to PCIe CN1
RX CAP on PCIe Slot Card.



Co-lay



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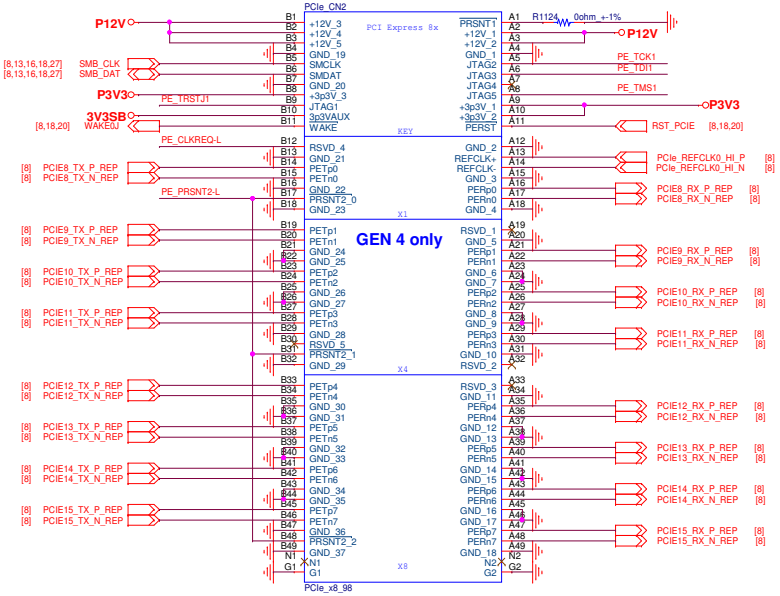
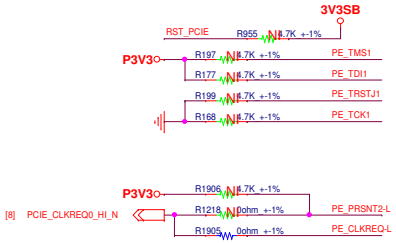
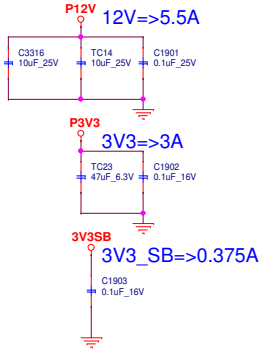
Title	PCI EXPRESS x4	
Size: B	Document Number: COM-HPC Mini Base	Rev: A1
Date: Wednesday, May 28, 2025	Sheet 18 of 43	

PCIe x8 Slot (PCIe 8-15)

TX CAP on Module
RX CAP on PCIe Slot Card.







Change to below part for Gen5
WIN WIN, WPEH-098AK1B3CHW8, Gen 5, open wall

Power Supply Rail Requirements

Power Rail	x1 Connector	x16 Connector
+3.3V		
Voltage tolerance	9%	9%
Supply Current	3.0 A	3.0 A
Capacitive Load	1000 uF	1000 uF
+12V		
Voltage tolerance	8%	8%
Supply Current	0.5 A	4.4 A
Capacitive Load	300 uF	2000 uF
+3.3Vaux		
Voltage tolerance	9%	9%
Supply Current		
Wakeup Enabled	375 mA	375 mA
Non-wakeup Enabled	20 mA	20 mA
Capacitive Load	150 uF	150 uF
	25 W	60 W

The power supply rails available at the PCI Express connectors, based on the number of PCI Express lanes supported by the connectors.

Table 4-1: Power Supply Rail Requirements

Power Rail	10 W Slot	25 W Slot	150W-ATX Power Connector	75 W Slot
+3.3V				
Voltage tolerance	± 9% (max)	± 9% (max)	N/A	± 9% (max)
Supply Current	3.0 A (max)	3.0 A (max)		3.0 A (max)
Capacitive Load	1000 µF (max)	1000 µF (max)		1000 µF (max)
+12V				
Voltage tolerance	± 8%	± 8%	+5% / -8% (max)	± 8%
Supply Current	0.5 A (max)	2.1 A (max)		5.5 A (max)
Capacitive Load	300 µF (max)	1000 µF (max)	6.25 A (max)	2000 µF (max)
+3.3Vaux			N/A	
Voltage tolerance	± 9% (max)	± 9% (max)		± 9% (max)
Supply Current				
Wakeup Enabled	375 mA (max)	375 mA (max)		375 mA (max)
Non-wakeup Enabled	20 mA (max)	20 mA (max)		20 mA (max)
Capacitive Load	150 µF (max)	150 µF (max)		150 µF (max)

Notes:
1. The maximum current slew rate for each add-in card shall be no more than 0.1 A/µs.
2. Each add-in card shall limit its bulk capacitance on each power rail to less than the values shown in Table 4-1.
3. System boards that support Hot-Plug add-in cards shall limit the voltage slew rate so that the inrush current to the card shall not exceed the specified maximum current. This is calculated by the equation dV/dt = I/C; where:
   I = maximum allowed current (A)
   C = maximum allowed bulk capacitance (F)
   dV/dt = maximum allowed voltage slew rate (V/s)
4. The maximum voltage variation between +12V inputs is 1.92 V.

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Title: PCI EXPRESS x8
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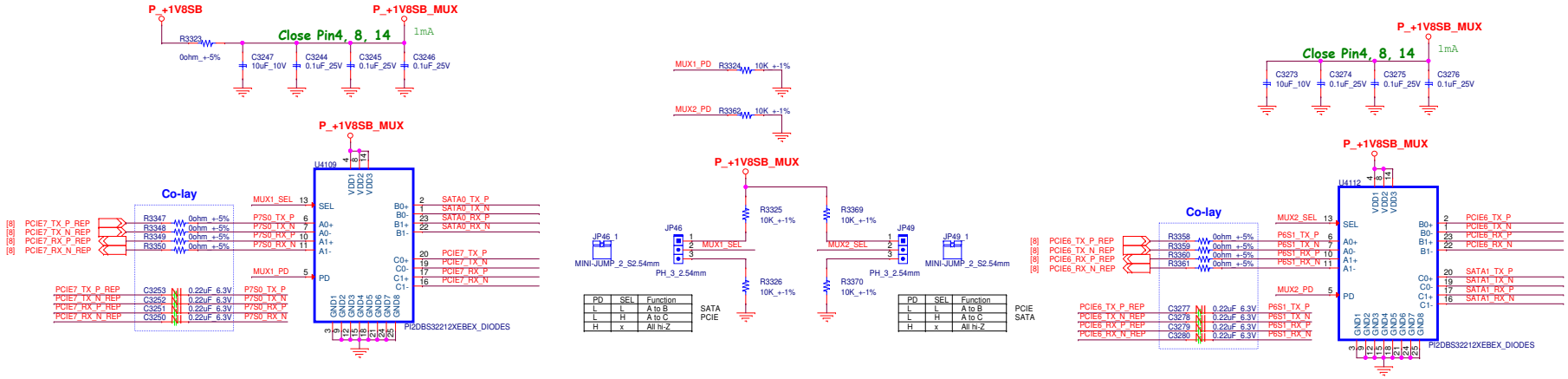
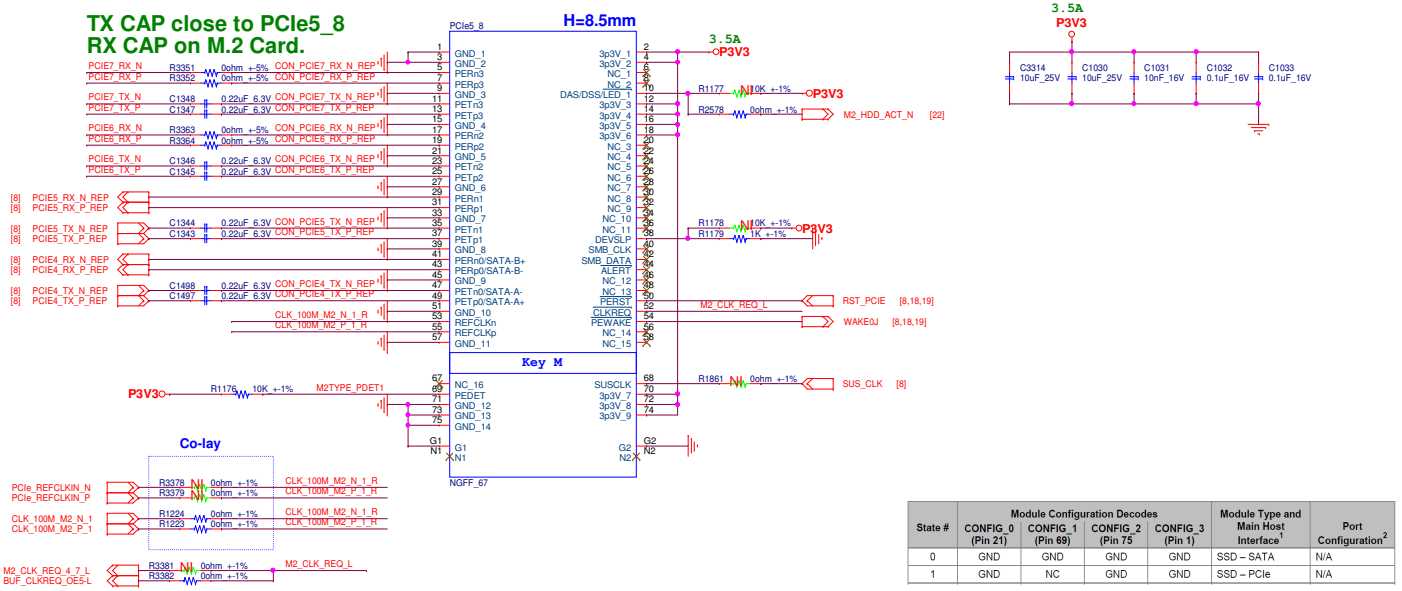
PCIE/SATA Switch

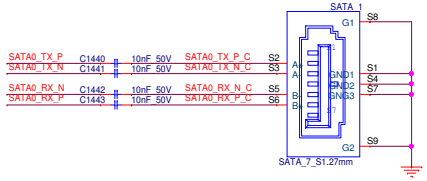


M.2 key-M Slot 1 (PCIE 4-7 Gen5)

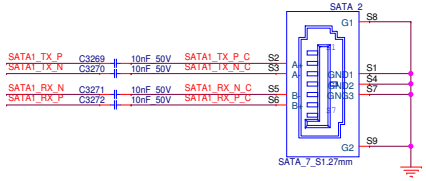


State #	Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	NC	GND	GND	SSD – PCIe	N/A

SATA 0



SATA 1



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Title: M.2 Key-M Slot/SATA

Size: C | Document Number: COM-HPC Mini Base | Rev: A1

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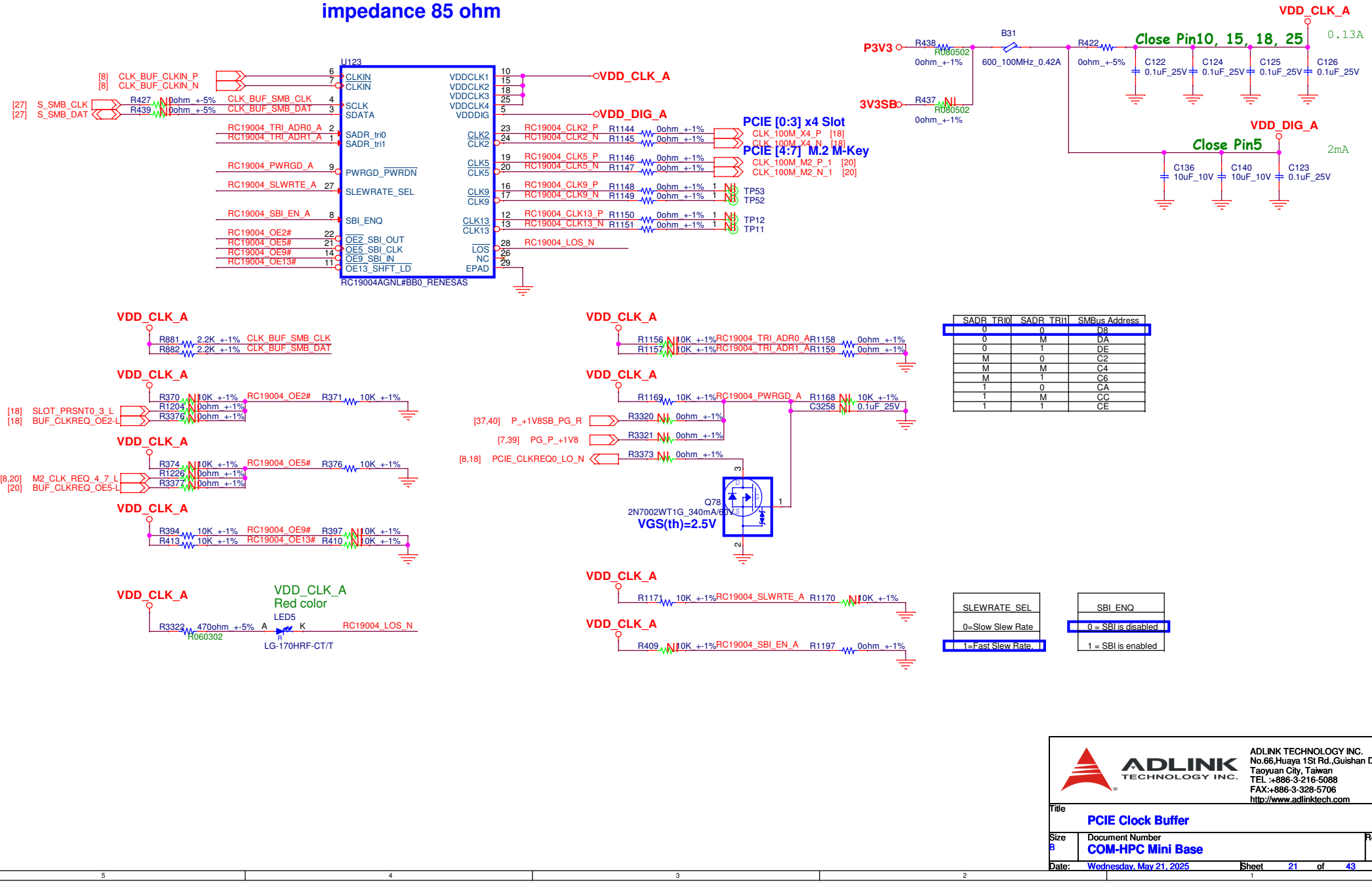
impedance 85 ohm
U123
RC19004AGNL#BB0_RENESAS
PCIE [0:3] x4 Slot
PCIE [4:7] M.2 M-Key
VDD_CLK_A
VDD_DIG_A
Close Pin10, 15, 18, 25
0.13A
Close Pin5
2mA
P3V3
3V3SB
B31
600_100MHz_0.42A
VDD_CLK_A
Red color
LED5
LG-170HRF-CT/T
Q78
2N7002WT1G_340mA/60V
VGS(th)=2.5V
SADR_TRI0 SADR_TRI1 SMBus Address
0 0 D8
0 M DA
0 1 DE
M 0 C2
M M C4
M 1 C6
1 0 CA
1 M CC
1 1 CE
SLEWRATE_SEL
0=Slow Slew Rate
1=Fast Slew Rate
SBI_ENQ
0 = SBI is disabled
1 = SBI is enabled
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Title
PCIE Clock Buffer
Size B
Document Number
COM-HPC Mini Base
Rev A1
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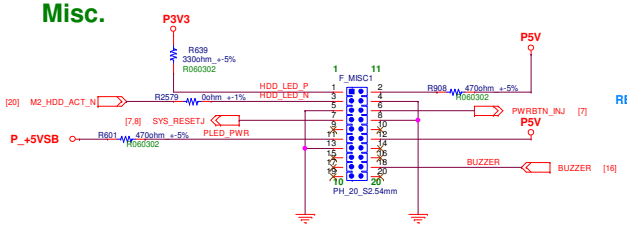
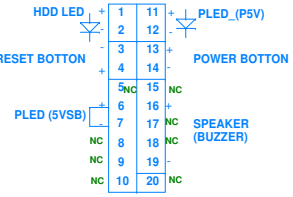
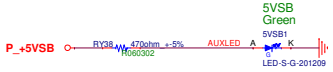
Misc.



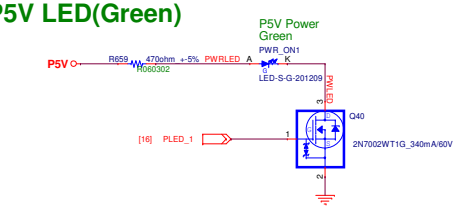
Miscellaneous Pin Header



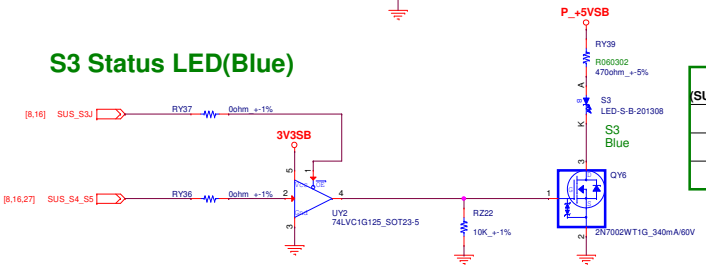
Module 5V Status LED(Green)



P5V LED(Green)

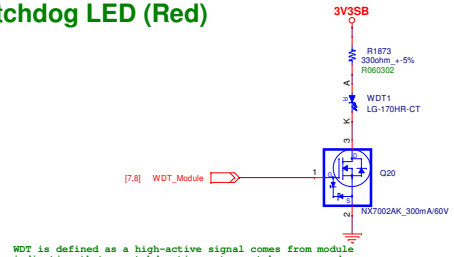


S3 Status LED(Blue)



OE# (SUS_S3J)	A (SUS_S4J)	Output Y
L	H	H
L	L	L
H	X	Z

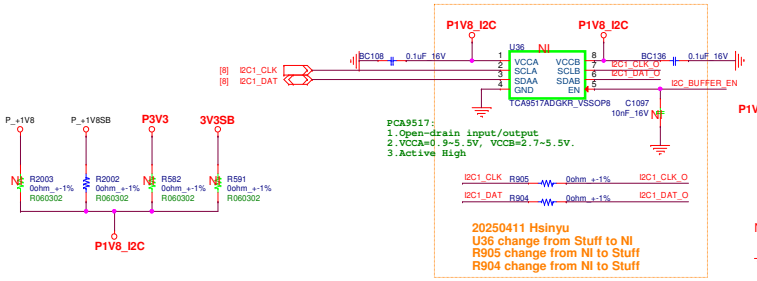
Watchdog LED (Red)

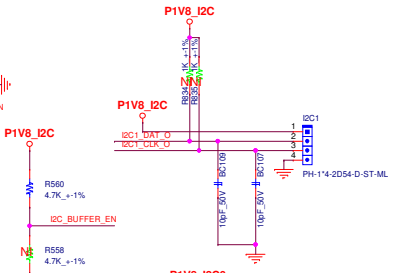


WDT is defined as a high-active signal comes from module indicating that a watchdog time-out event has occurred.

I2C1

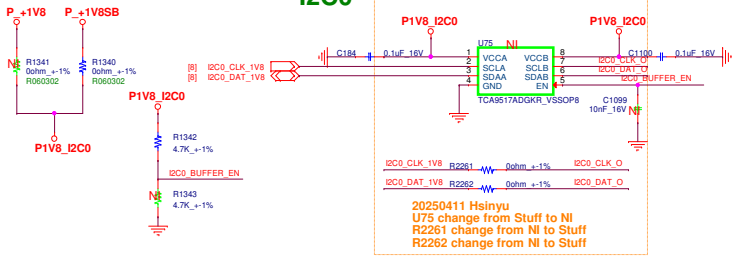
I2C BUFFER

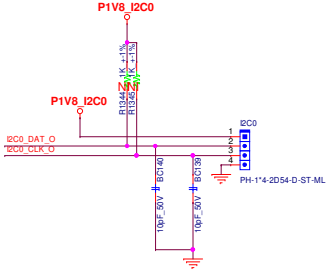




I2C0

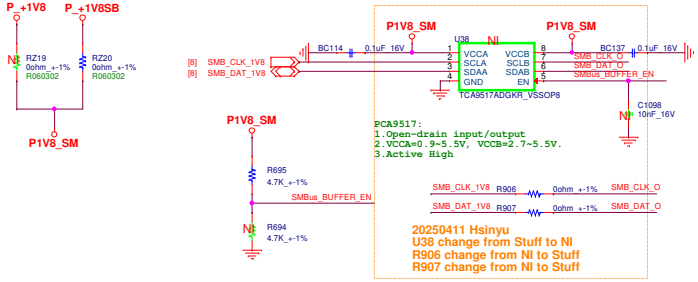
I2C0 BUFFER

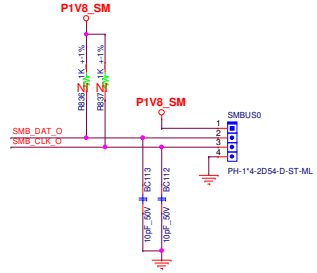




SMBus

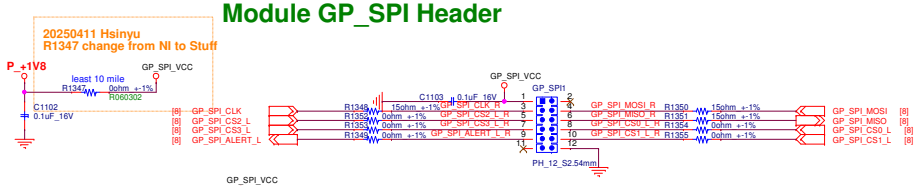
SMBus BUFFER

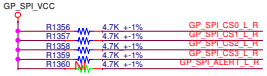




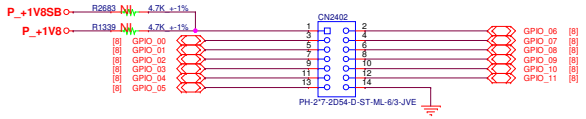
Module GP_SPI Header

20250411 Hsinyu
R1347 change from NI to Stuff





Module GPIOs



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Title	Misc. & GPIOs & GP SPI	
Size: A2	Document Number: COM-HPC Mini Base	Rev: A1
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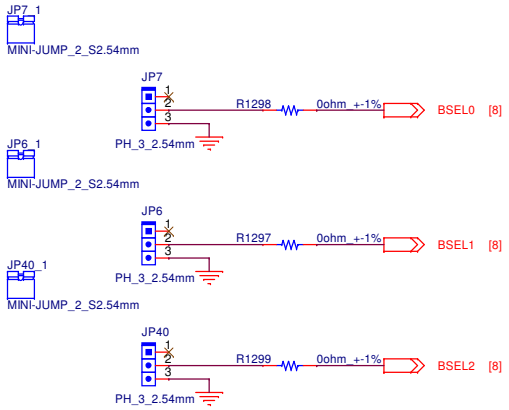
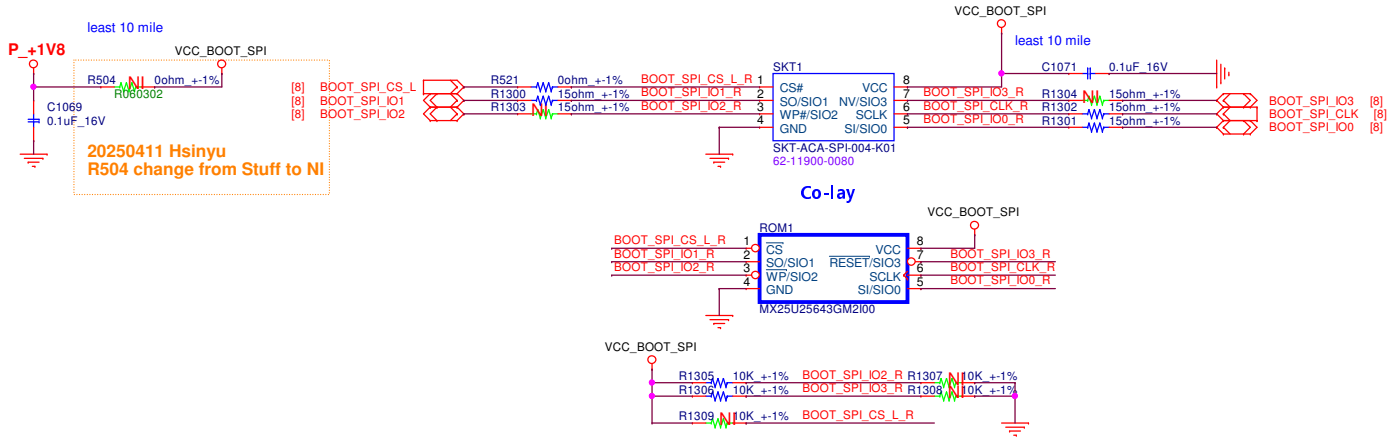
BSEL [0:2] Pulled up on Module to vendor specific power rail



Ref	BSEL[2:0]	Chipset eSPI_CS2# If Available on chipset	Chipset eSPI1_CS1# If Available on chipset	Chipset eSPI0_CS0#	Chipset SPI_CS1#	Chipset SPI_CS0#	Boot Option	Boot Option and CS# Routing Details	Use Case
7a	111	Carrier J1.B55 COM-HPC eSPI_CS1#	Carrier J1.B54 COM-HPC eSPI_CS0#	Module	Module	Module	MAFS on Module	CSME / DT on Chipset SPI0 device on Module BIOS on SPI0 or SPI1 on Module	Most Common Usage
7b							SAFS on Module	CSME / DT on Slave Attached Flash on Module BIOS on Module SAFS	Module EC/MMC with SAFS BIOS on far side of EC/MMC
6	110	Carrier J1.B55	Carrier J1.B54	Module	Module	Carrier J1.B48	MAFS on Carrier	CSME / DT on Chipset SPI0 device on Carrier BIOS on SPI0 on Carrier or on SPI1 on Module	Casino Gaming Removable BIOS option on Carrier
5	101	Carrier J1.B55	Carrier J1.B54	Module	Carrier J1.B48	Module	MAFS on Module	CSME / DT on Chipset SPI0 device on Module BIOS on SPI0 on Module or on SP1 on Carrier	Casino Gaming Removable BIOS option on Carrier Alternate version
4	100								Spare – reserved for future use
3	011	Carrier J1.B55	Module	Carrier J1.B54 COM-HPC eSPI_CS0#	Module	Module	MAFS on Module	CSME / DT on Chipset SPI0 device on Module BIOS on SPI0 or SPI1 on Module	Same as Ref 7a except eSPI_CS routing
2	010	Carrier J1.B55	Module	Carrier J1.B54	Module	Module	SAFS on Carrier	CSME / DT on Carrier SAFS BIOS on Carrier SAFS	BIOS totally under Carrier BMC control
1	001	Carrier J1.B55	Module	Carrier J1.B54	Module	Module	MAFS on Module and SAFS on Carrier	CSME / DT on Chipset SPI0 device on Module BIOS on Carrier SAFS	BIOS mostly under Carrier BMC control
0	000								Spare – reserved for future use

SPI BOOT



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Title: SPI BOOT & SEL

Size: A3 | Document Number: COM-HPC Mini Base | Rev: A1

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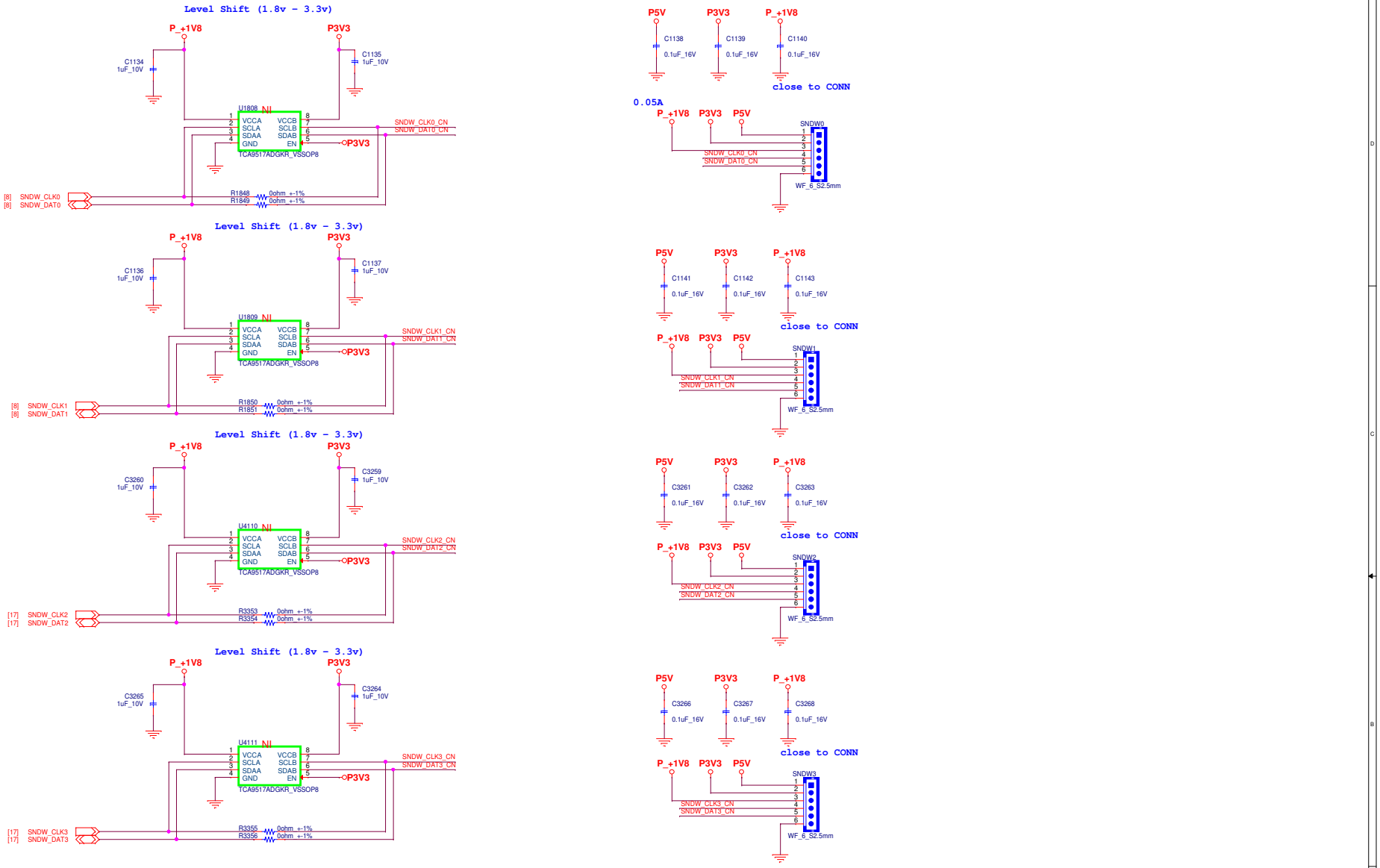
Sound Wire



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Title	Sound Wire0/1	
Size: C	Document Number: COM-HPC Mini Base	Rev: A1
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Title

Reserved

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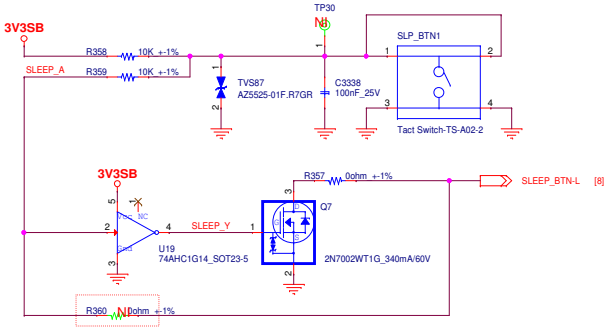
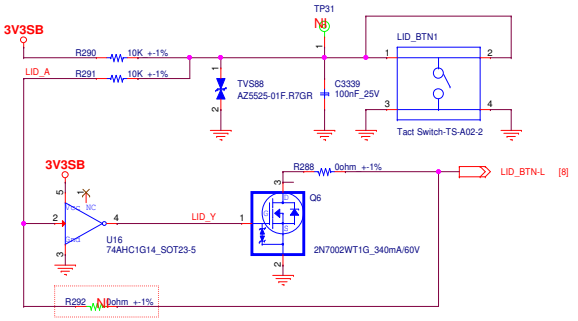
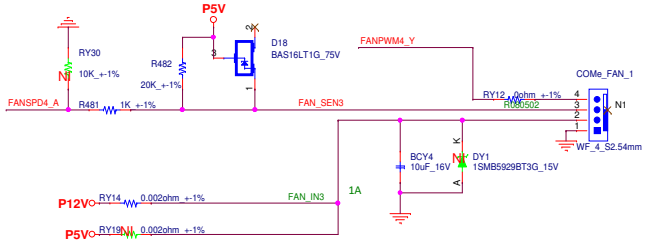
SLEEP BTN

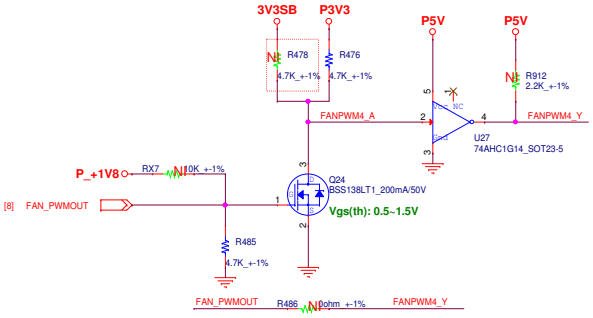


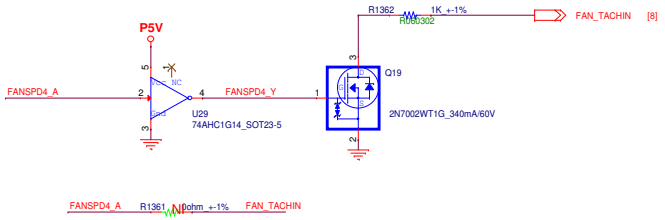
LID BTN



FAN (from module)







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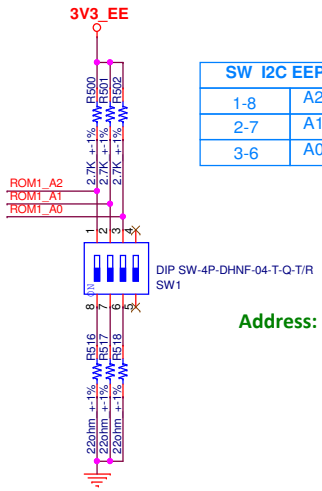
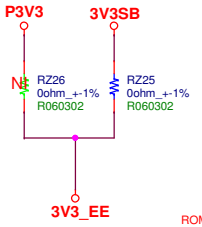
Title	Module FAN & LID/Sleep BTN	
Size: C	Document Number: COM-HPC Mini Base	Rev: A1
Date: Wednesday, May 21, 2025	Sheet 26 of 43	

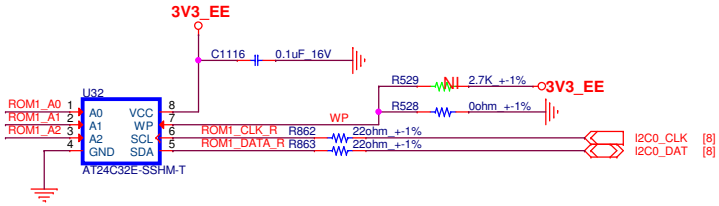
I2C EEPROM



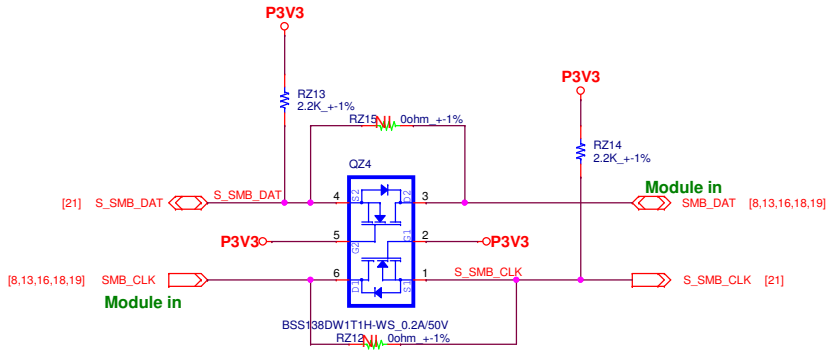
SW I2C EEPROM_U32	
1-8	A2_ON (LOW)
2-7	A1_OFF (High)
3-6	A0_ON (LOW)

Address: A4h



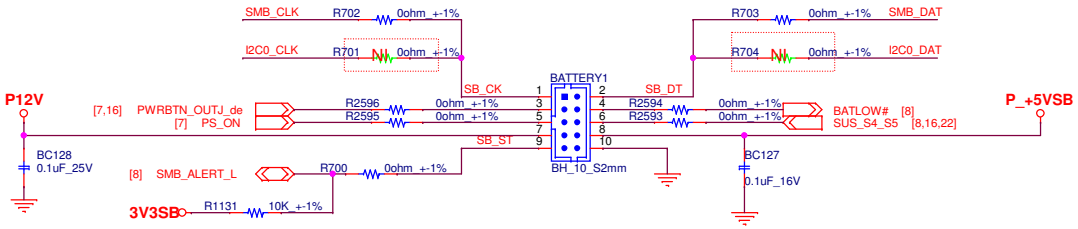


Package	Device Type Identifier				Hardware Client Address Bits			R/W Select
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SOIC, TSSOP, UDFN, VFBGA	1	0	1	0	A2	A1	A0	R/$\overline{W}$



Samrt Battery

CAUTION!!
20250411 Hsinyu
Need to re-design 1.8V to 3.3V level shift to support Smart Battery function.



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Title	I2C EEPROM / SMBUS	
Size: Custom	Document Number: COM-HPC Mini Base	Rev: A1
Date: Friday, January 09, 2026	Sheet 27 of 43	

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Title

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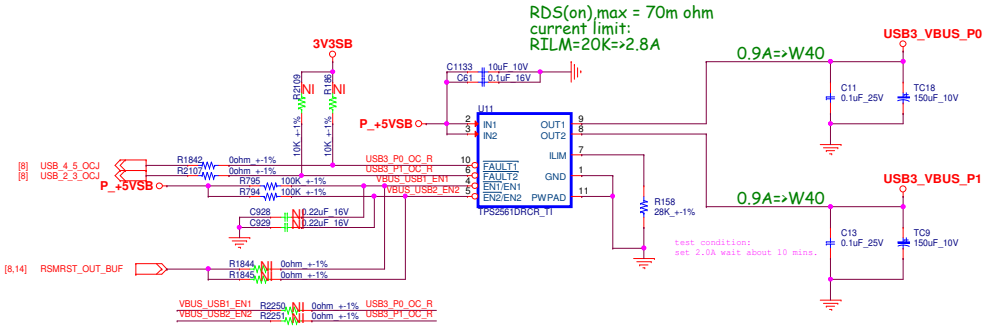
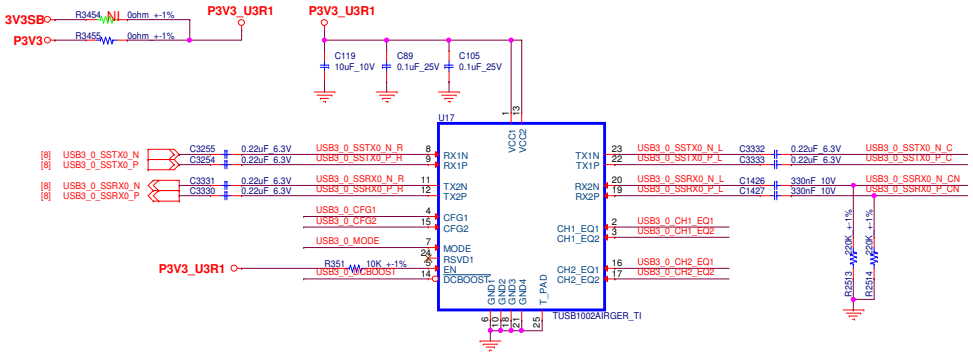
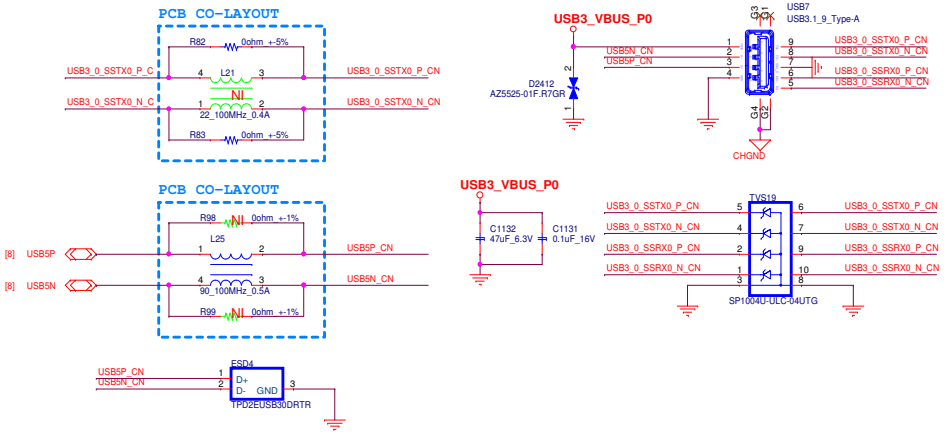


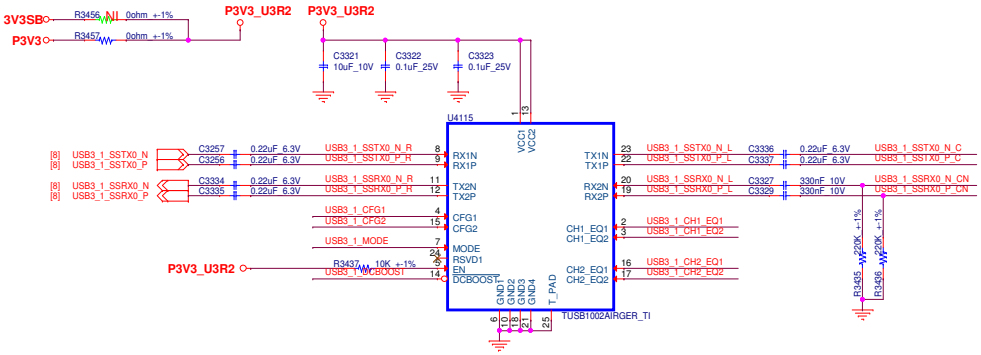
DEVICE (1)	AMBIENT TEMPERATURE (2)	ENABLE	SON (3) (DRC)	MARKING	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT PER CHANNEL
TPS2560	–40°C to 85°C	Active low	TPS2560DRC	2560	2.5 A
TPS2561		Active high	TPS2561DRC	2561	

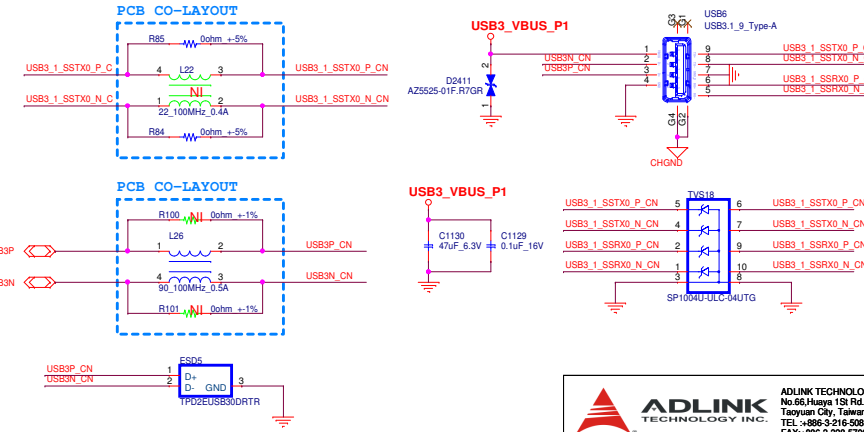
USB 3.2 Port 0





USB 3.2 Port 1





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Title: USB3.2 Gen2_Rear IO

Size: C | Document Number: COM-HPC Mini Base | Rev: A1

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C	COM-HPC Mini Base	A1

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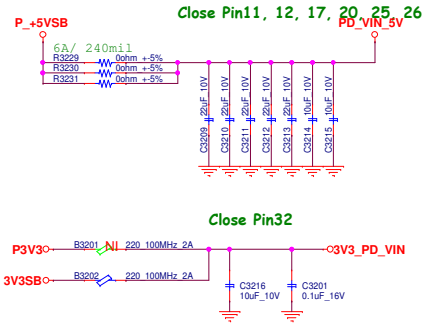
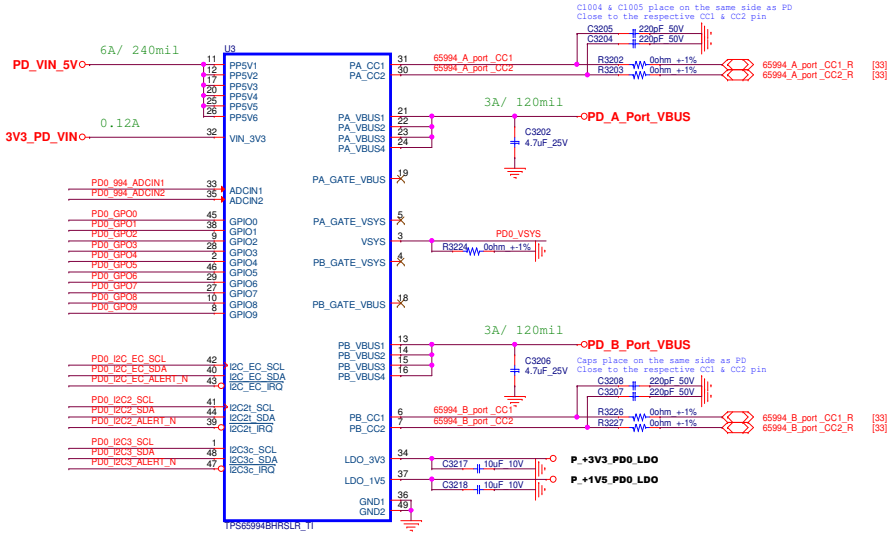
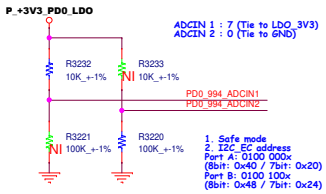
TPS65994 PD 2Port



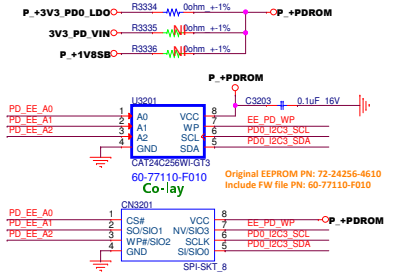


Mode and I2C_EC address setting

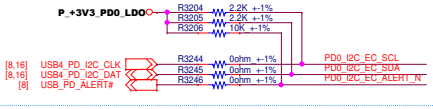


DIV			
MIN	Target	MAX	ADCINx decoded value
0	0.0114	0.0228	0
0.0229	0.0475	0.0722	1
0.0723	0.1074	0.1425	2
0.1425	0.1899	0.2372	3
0.2373	0.3022	0.3671	4
0.3672	0.5358	0.7064	5
0.7065	0.8062	0.9060	6
0.9061	0.9530	1.0	7

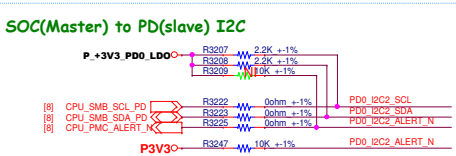
I2C EEPROM



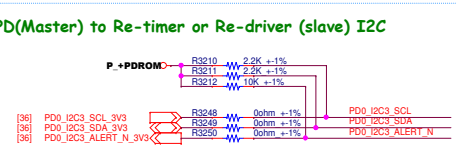
EC(Master) to PD(slave) I2C



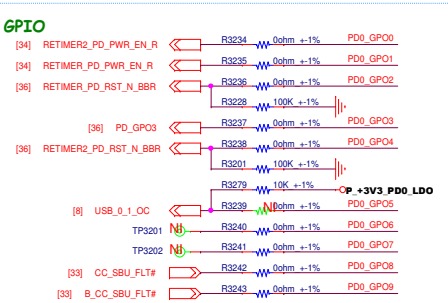
SOC(Master) to PD(slave) I2C



PD(Master) to Re-timer or Re-driver (slave) I2C



GPIO



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Title: PD_TPS65994BH_2 Port

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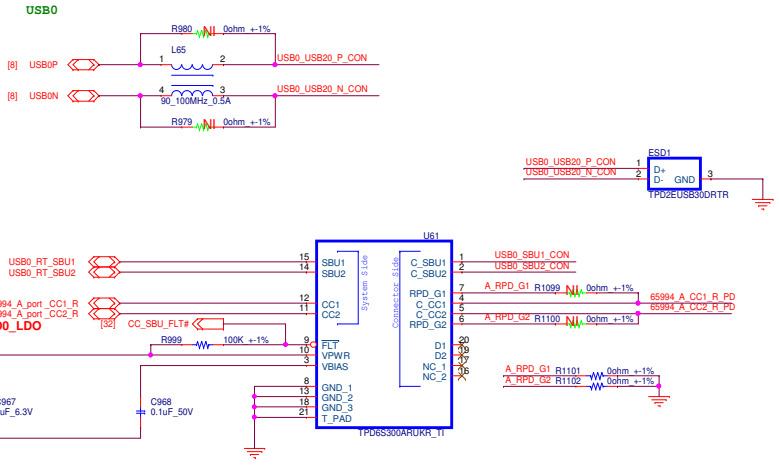
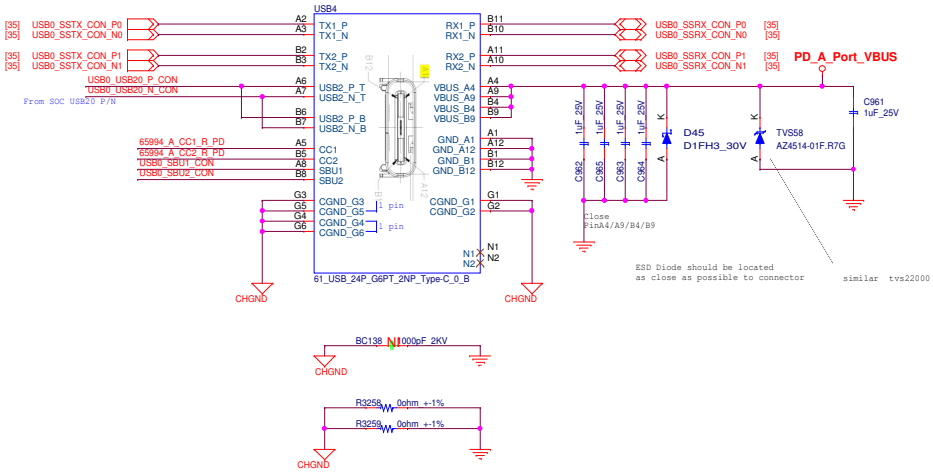
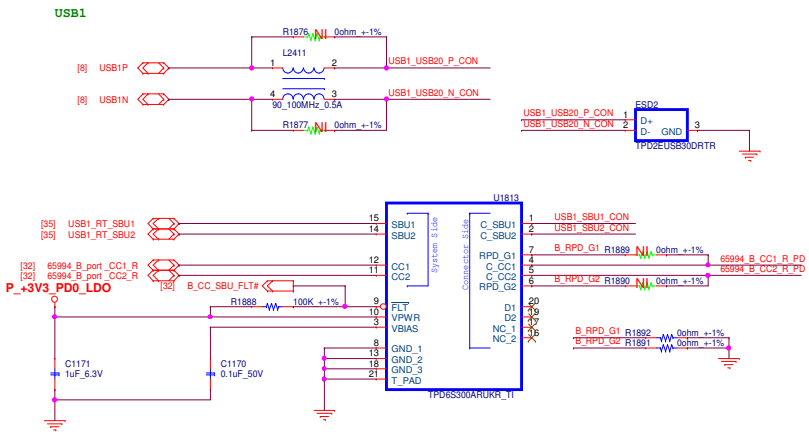
USB0 For USB4 HBR0 Retimer

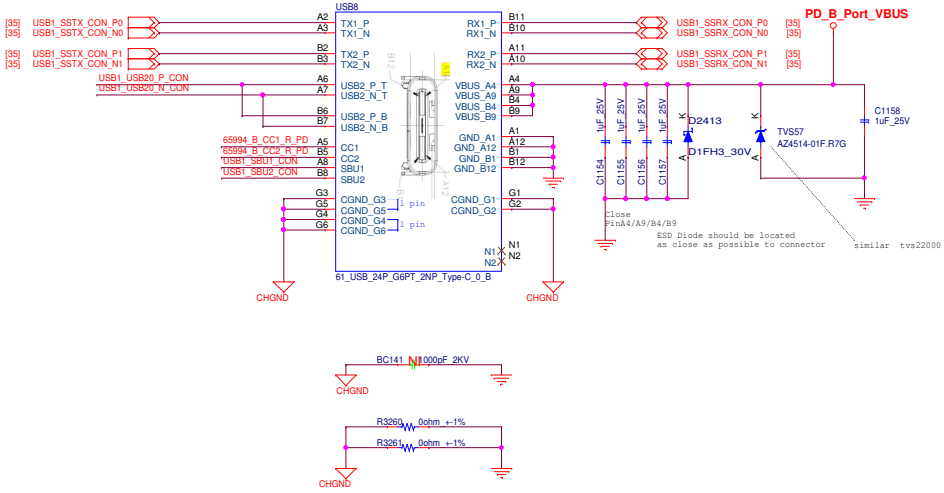


Type-C Connrctor useing 61-G2621-0240 , PM decide to this connector solution



USB1 For USB4 HBR1 Retimer





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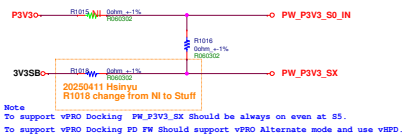
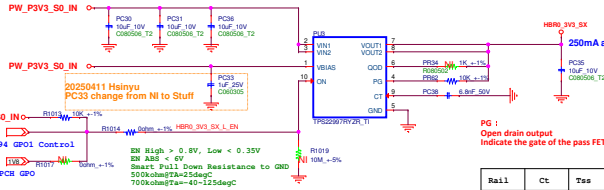
Title	USB Type-C 2port	
Size: C	Document Number: COM-HPC Mini Base	Rev: A1
Date: Wednesday, May 21, 2025	Sheet 33 of 43	



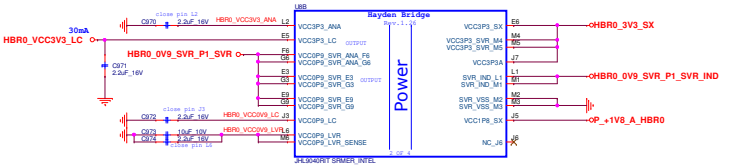
Note
To support vPRO Docking PW_P3V3_SX Should be always on even at S5.
To support vPRO Docking PD FW Should support vPRO Alternate mode and use vHPD.

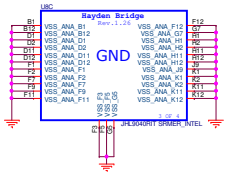
TPS22997
VIN range 0.1V~5.5V
Vbias range 1.5V to 5.5V
Maximum continuous current 10A
Ron = 4.0mohm(typ)
Adjustable slew rate control
Adjustable quick output discharge (QOD)
Open drain Power Good (PG) signal
Thermal shutdown (150~190degC)
Thermal shutdown hysteresis 20degC
WQFN 1.5mm*2.0mm
JA=83.7degC/W

TPS22997 power sequence
1. VIN
2. VBIAS
3. ON/PG
4. Output



Rail	Ct	Tss	Co_max for inrush<0.5A	Co_max for inrush<1.5A
3.30V	6.8nF	3.087mS	467.7uF	1403.1uF





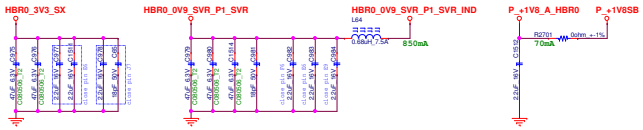


Figure 7. Power On Sequence

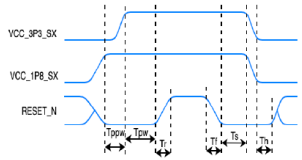
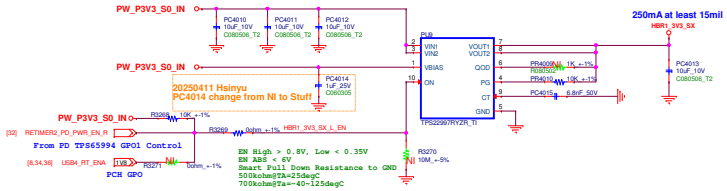
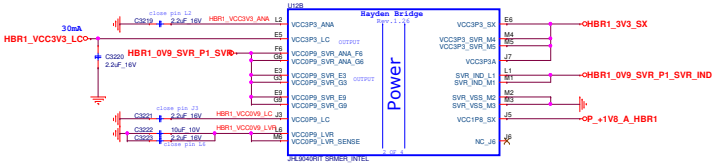
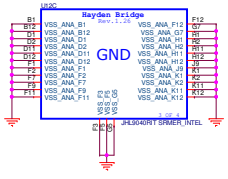


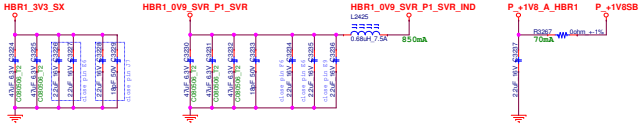
Table 13. Power On Sequence timing parameters

Parameter	Description	Min	Max	Units
Tpw	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us
T_{ppw}	From VCC1P8_SX at 90% to VCC3P3_SX at 90%	0	-	ns
Tr~Tf	RESET_N rise/fall time	0.1	500	ns
Ts	RESET_N setup time prior to VCC_3P3_SX disconnect	500	-	ns
Th	RESET_N hold time after VCC_3P3_SX disconnect	0.1	-	ns









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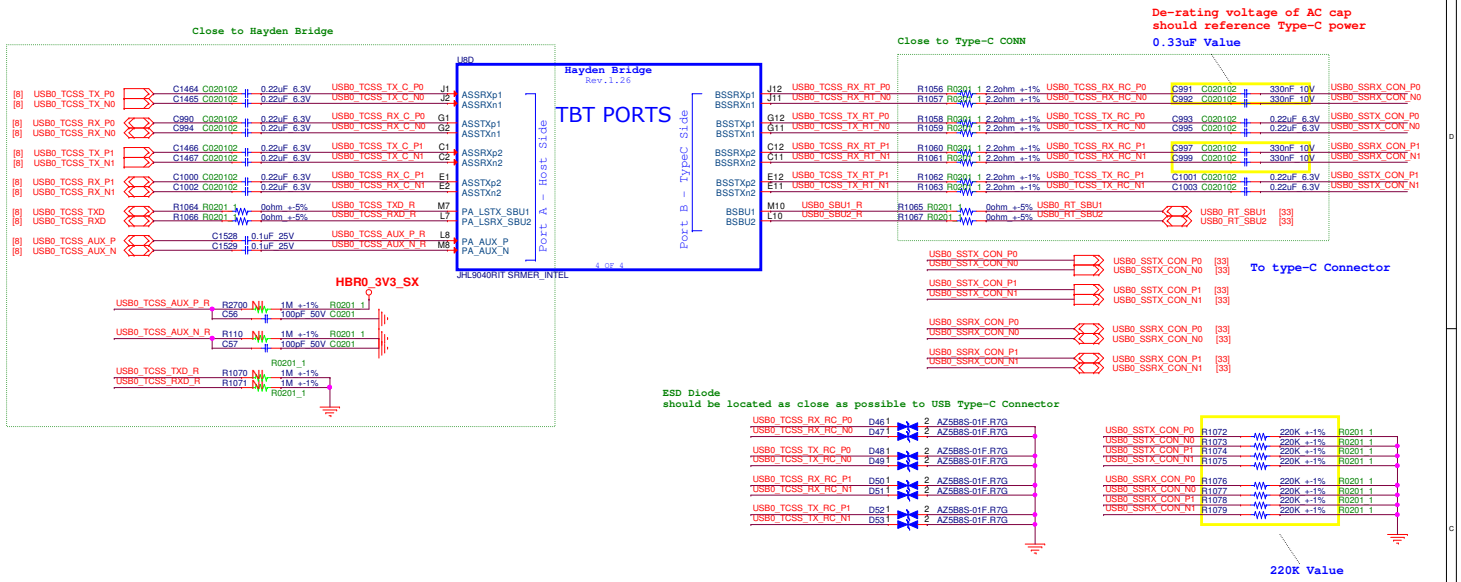
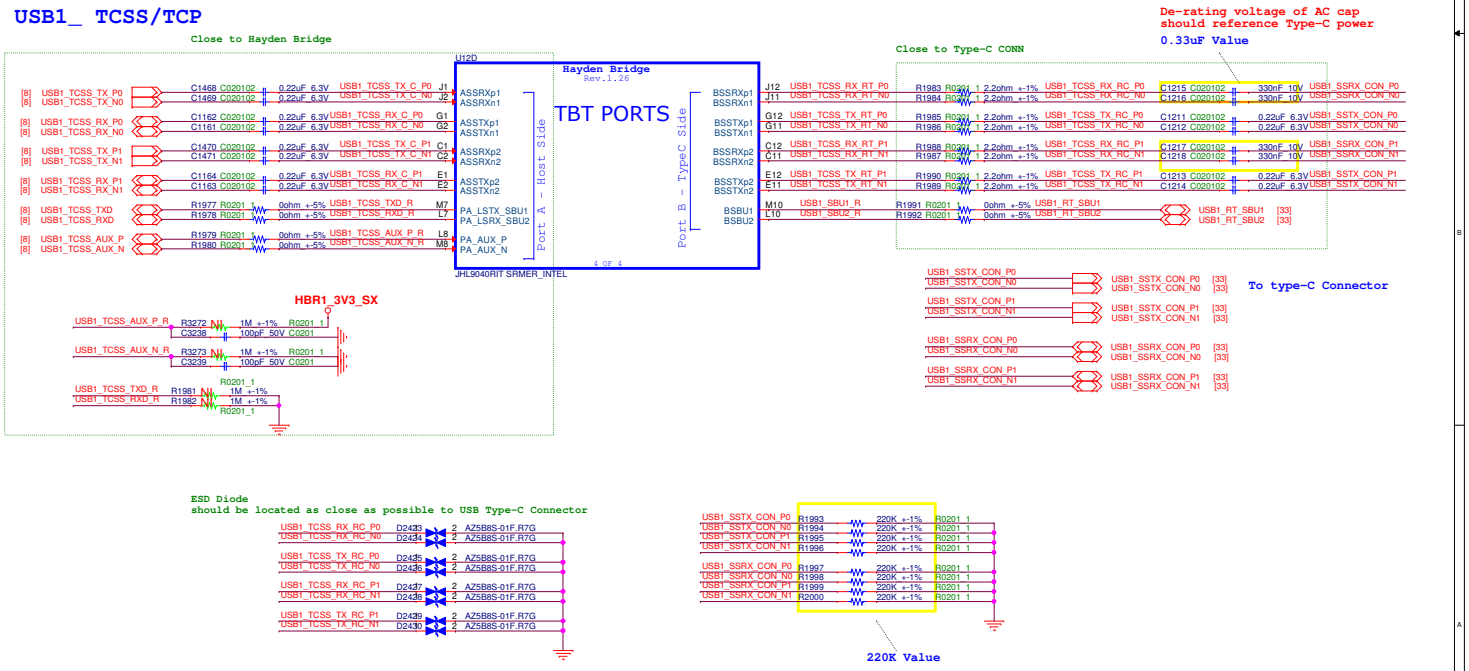
Title: Hayden Bridge_POWER/GND
Size: Custom | Document Number: COM-HPC Mini Base | Rev: A1
Date: Wednesday, May 21, 2025 | Sheet 34 of 43

USB0_ TCSS/TCP



USB1_ TCSS/TCP



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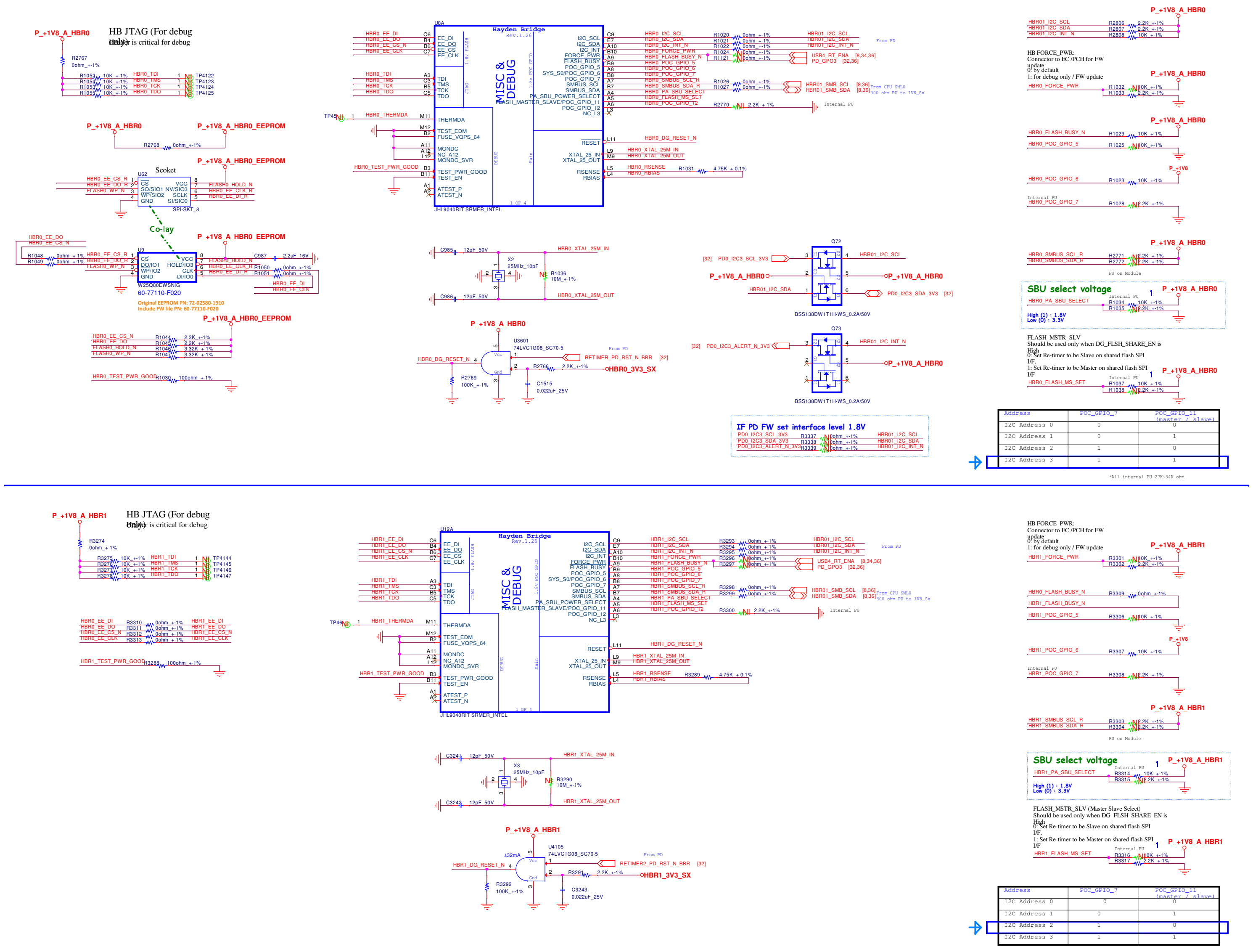
Title	Hayden Bridge_TBT Port	
Size: Custom	Document Number: COM-HPC Mini Base	Rev: A1
Date: Wednesday, May 21, 2025	Sheet 35 of 43	



Address	POC_GPIO_7	POC_GPIO_11 (master / slave)
I2C Address 0	0	0
I2C Address 1	0	1
I2C Address 2	1	0
I2C Address 3	1	1

*All internal PU 27K~34K ohm

Address	POC_GPIO_7	POC_GPIO_11 (master / slave)
I2C Address 0	0	0
I2C Address 1	0	1
I2C Address 2	1	0
I2C Address 3	1	1

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Title: Hayden Bridge_MISC_DEBUG

Size: D | Document Number: COM-HPC Mini Base | Rev: A1

Date: Wednesday, May 21, 2025

Power Source

Input -------->

8V~20V

7.4A@Vin=20V,eff97.3%,PD_Buck_H=0.838W,PD_Buck_L=0.282W/per

18.75A@Vin=8V,eff95.94%,PD_Buck_H=0.858W,PD_Buck_L=0.912W/per

PSU_+12V_Vin8-20V — PL513 0.1uH_3A8 (Cyntec HBTD042T-R10MS) — P_+12V_A_VINFLT_S

0.1uH34A/35A/1.3mohm/1.6mohm

4.3*4.3*2mm

VDD/Vdrv/Vbias -------->

Output <--------

P12V — P12V_

P12V(LT8390)

P_+12V Specification:
Vout: 12V
Imax: 12A /144W
Istep: 6A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 201kHZ

LT8390 Buck-boost controller
VIN range 4~60V
QFN 4mm x 5mm
JA=43degC/W

PSU_+12V_Vin8-20V — P12V — R1898 R1899 R1900 R1901 R1902 R1903 R1904 R1905 0.0005ohm_+-1%/R251204_3D68

25SVPF180M 8*11.9
ESR= 16mohm
Ripple current= 4650mA@100kHz

>880mil

PC112 PC111 PC110 180uF_25V SECAP_8X11D9 — PC1 0.1uF_50V C060304 — PC108 PC107 PC106 PC105 PC104 PC103 PC102 PC101 10uF_25V C080506_T2

PQ21 PQ22 BSC0906NS_63A/30V

2W PR18 3mohm_+-1% R251203_3D68

2W PR17 3mohm_+-1% R251203_3D68

Gotrend GSTL1770D-3R3M
3.3uH/30A/32A/2.7mohm/3.3mohm
17.8*16.9*6.7mm

PL4 3.3uH_30A

PSP1 PSP2 R6402_SHT_PAD

PQ23 BSC0901NS_100A/30V

PC18 0.1uF_50V C060304

PR83 0ohm_+-1% R060302

PR84 0ohm_+-1% R060302

PR86 1.5ohm_+-1% R251203

PC27 1000pF_100V C060304

PQ11 BSC0901NS_100A/30V

PR65 PR66 0ohm_+-1% R060302

PC1231 1uF_50V C080506_T2

PC1216 0.1uF_50V C060304

PR2019 1.5ohm_+-1% R251203

PR2004 0ohm_+-1% R060302

PC1218 1000pF_100V C060304

PR2007 0ohm_+-1% R060302

PQ19 PQ18 BSC0906NS_63A/30V

PQ19 PQ23 BSC0901NS_100A/30V

PR1894 0.001ohm_+-1% R251204

Current limit setting I_V_CTRL=0.5348V
OCP = (VCTRL - 0.25V) / (10* Rsense)
= (0.4607 - 0.25V) / (10* 1mohm)
=21.06A

PC1222 PC1175 PC1176 PC1177 10uF_25V C080506_T2 — PC1182 270uF_16V SECAP_6D3X10

PC1178 PC1179 PC1180 PC1181 PC1185 PC1186 PC1187 10uF_25V C080506_T2 — 270uF_16V SECAP_6D3X10

>480mil — 12A — P12V

16SVPG270M,6.6*6.9mm
ESR= 8mohm
Ripple current= 5800mA@100kHz

PSP4 PSP3 R6402_SHT_PAD

PC1230 1uF_16V C060304

PR1899 0ohm_+-1% P_+12V_A_Vout_R

PR1902 20ohm_+-1% R060302

PR22 118K_+-1%

PR25 10.7K_+-1%

PC1237 47pF_50V

PC1240 47pF_50V

Vout
=1/10.7K*(10.7K+118K)
=12V

PC1229 1uF_16V

PR1900 PR1901 10ohm_+-1%

PR24 PR26 0ohm_+-1%

P_+12V_A_INTVCC

INTVCC=5V

PC1236 4.7uF_10V C060304

LOADTG/LOADEN
If the load switch control is not used, tie this pin to VREF or INTVCC

VCTRL > 1.35V, the current sense threshold is constant at 195mV full scale value.
VCTRL= Vref*Rb / (Ra + Rb)
= 2 * 0.2k (27.4k +8.2k)
= 0.4607V

For parallel applications, tie the master LT8390 ISMON pin to the slave LT8390 CTRL pin.

Vref=2V — PR27 27.4K_+-1% — PR1895 8.2K_+-1% — PC1217 0.47uF_16V C060305 — PC1173 0.1uF_16V C060305

tSS = 1V*(CSS/12.5uA) ~1*(0.1/12.5) = 8mS

PC1239 68pF_50V — PR2022 32.4K_+-1% — PC1242 4700pF_50V — PR2010 221K_+-1% Frequency=200kHz

LT8390IUF#PBF_ADI

EN

LT8390 power sequence
1. PIN4 VIN
2. PIN5 INTVCC(Internal LDO)
3. PIN6 EN
4. Output
5. PIN14 PG (Active low)

P_+12V_A_VINFLT_S — Rau PR4618 374K_+-1% — EN P_+12V_A_RS — PR4617 0ohm_+-1% — P_+12V_A_EN_UVLO — Rbu PR4619 120K_+-1% — PC8394 1uF_50V

RUN Pin

LT8390_RUN Pin
Absolute Value:60V to -0.3V
On-Threshold:1.22V(VIN=7.9V)

Absolute Value:60V to -0.3V
On-Threshold:1.22V(VIN=5.02V)

Enable option 1

PG

P_+12V_A_INTVCC — PR4621 100K_+-1% — [38] P_+12V_A_PG_R — P_+12V_A_PG_R — PR4620 200K_+-1%

NOTICE:
PGOOD is inverse.

P_+1V8SB_PG Control 12V_EN (Default)

P_+12V_A_VINFLT_S — R2761 30.1K_+-1% — R2760 10K_+-1% — R1936 9.09K_+-1% — R1935 365K_+-1%

[21,40] P_+1V8SB_PG_R — R2763 0ohm_+-1% — 2N7002WT1G_340mA/60V Q69 — PR1926 0ohm_+-1% — R060302 — P_+12V_A_EN_UVLO

R2762 12.1K_+-1% — C1192 0.1uF_16V — 2N7002WT1G_340mA/60V Q67 — PR1925 0ohm_+-1% — R060302 — R2001 120K_+-1% — PC1208 1nF_50V

Power good pin is OPEN-DRAIN
Vmax<6V

RUN Pin
8V Div>=1.95V
20V Div>= 4.85V

Enable option 2

P_+1V8SB_PG Control 12V_EN (without UVLO)

P_+12V_A_INTVCC — R2764 10K_+-1% — P_+1V8SB_PG_R — R2765 0ohm_+-1% — P_+12V_A_EN_UVLO

Enable option 3

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Title	8-20VIN_P_+12V-LT8390	
Size: D	Document Number: COM-HPC Mini Base	Rev: A1
Date: Wednesday, May 21, 2025	Sheet 37 of 43	

Power Source

Input --------> 12V
9.1176@Vin=12V,85%eff

Cyntec HBTD042T-R10MS
0.1uH/34A/35A/1.3mohm/1.6mohm
4.3*4.3*2mm

PSU_+12V_Vin8-20V — PL509 0.1uH_34A — P_+5V_3V3_VINFIT

VDD/Vdrv/Vbias --------->

Output <---------
P_+5VSB
P3V3

EN TPS51225B power sequence
1. VIN
2. VREG3(internal LDO)
3. EN
4. Output

EN High>1.6V, Low<0.3v
EN Abs<5.5v

P_3V3_LDO — PR4608 10K_+-1% — PR4609 10K_+-1% — P_5V_A_EN_R
[38] P5V_PGOOD — PR4599 0ohm_+-1% — EN_P3V3_A

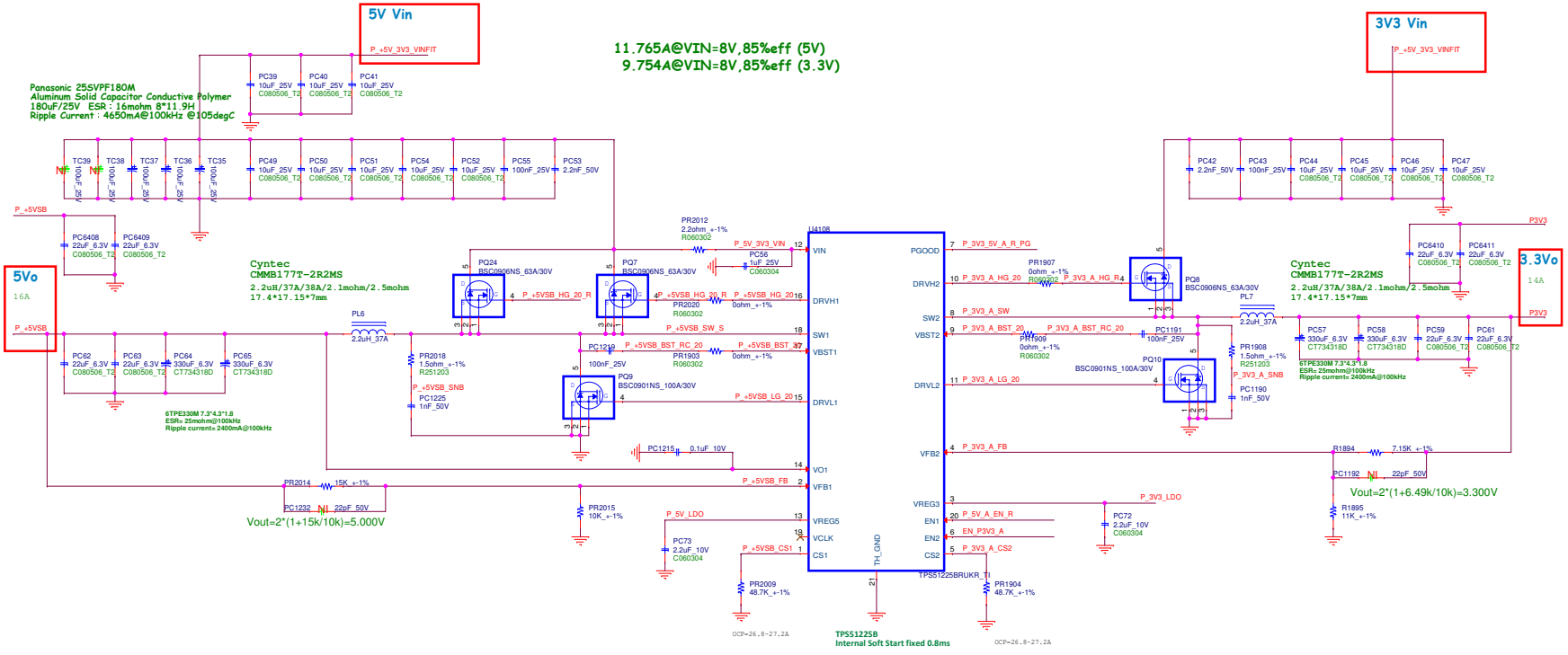
PG

P_3V3_LDO — PR4604 100K_+-1%
P_3V3_5V_A_PG — PR4607 0ohm_+-1% — P_3V3_5V_A_R_PG
PC6391 10nF_50V

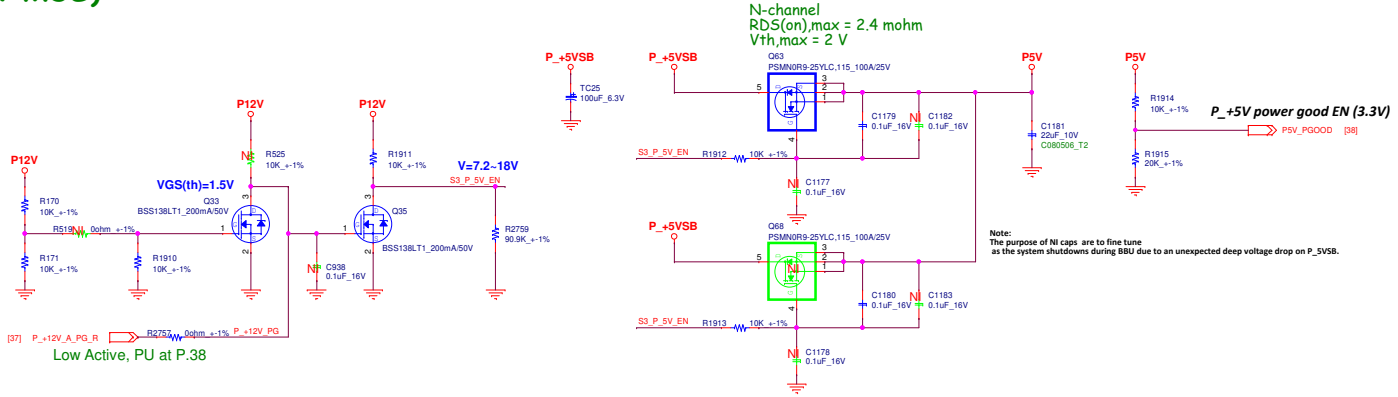
P_+5V_A/P_+3V3(TPS51225B)

P_+5V_A VR Specification:
Vout: 5.0V
Imax: 16A
Istep: 8A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 300kHZ

P_+3V3 VR Specification:
Vout: 3.3V
Imax: 14A
Istep: 7A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 355kHZ



P5V(N-MOS)



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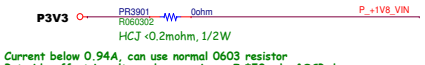
Title	8-20V_3V5V/20A/16A-TPS51225	
Size: A2	Document Number: COM-HPC Mini Base	Rev: A1
Date: Wednesday, May 21, 2025	Sheet 38 of 43	

Power Source

Input -------->

3.3V

1.169A@Vin=3.3V, eff93.41%,PD=0.254W

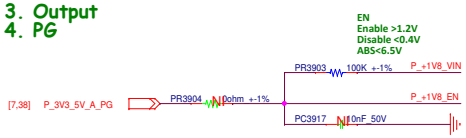


Current below 0.94A, can use normal 0603 resistor
But side effect is voltage drop maximum=Io*50mohm&OCP damage

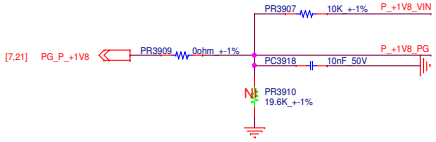
Output <---------

EN

MPM3840 power sequence
1. VIN
2. EN
3. Output
4. PG



PG



MPM3840 Pin14, PG internal pull high 500kohm
from VIN
Parallel external 10k, Rth=9.8kohm
If Vin = 5V0, insert 19.6kohm for Vpg=3.33V
If Vin = 3V3, No insert 19.6kohm for Vpg =Vin

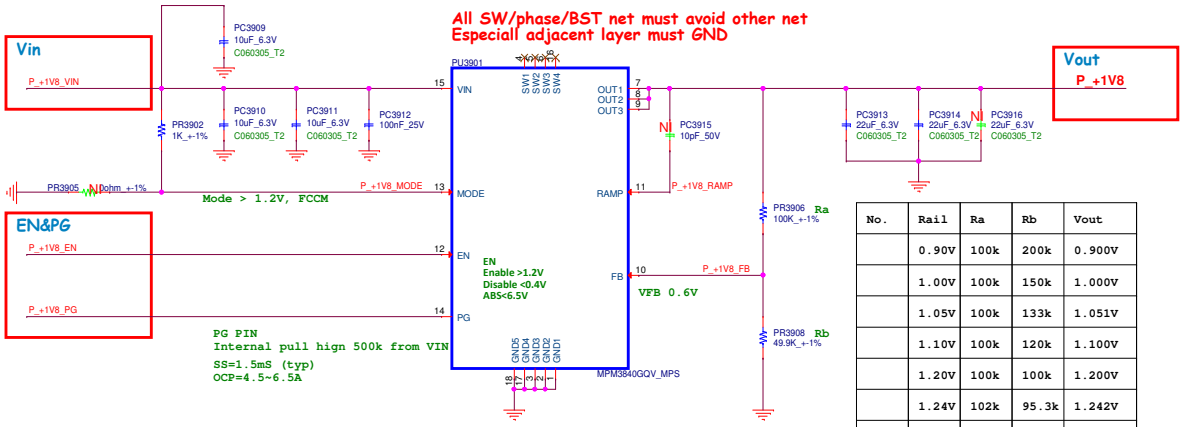
PG notes
1. Do loading PG
2. Recommend insert 10k, increase sink cability
3. If PG sink cability not enough,
please adjust divider resistance

P_+1V8 (MPM3840)

P_+1V8 Specification:
Vout: 1.8V
Imax: 2.0A
Istep: 1.0A
Slew Rate: 2.5A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 1.2MHZ

MPM3840
VIN range 2.8~5.5V
Io maximum 4.0A
QFN 3.0mm x 5.0mm x 1.6mm (chock inside)
JA(JESD51-7)=46degC/W
JA(70%)=32.2degC/W
Thermal evaluate by JA(70%)

All SW/phase/BST net must avoid other net
Especiall adjacent layer must GND



No.	Rail	Ra	Rb	Vout
	0.90V	100k	200k	0.900V
	1.00V	100k	150k	1.000V
	1.05V	100k	133k	1.051V
	1.10V	100k	120k	1.100V
	1.20V	100k	100k	1.200V
	1.24V	102k	95.3k	1.242V
	1.50V	100k	66.5k	1.502V
	1.70V	86.6k	47k	1.709V
*	1.80V	100k	49.9k	1.802V
	2.50V	105k	33k	2.509V
	2.57V	52.3k	16k	2.561V
	3.30V	102k	22.6k	3.308V

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Title: Power_P_+1V8

Size: C | Document Number: COM-HPC Mini Base | Rev: A1

Date: Wednesday, May 21, 2025 | Sheet 39 of 43

Power Source

Input -------->

5V

PD calculation deduct DCR loss (Io*Io*DCR 16mohm)

1.438A@Vin=5.0V, eff96.4%,PD=0.259W

Output <--------

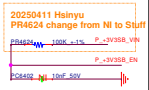
3V3SB

EN

MP2145 power sequence

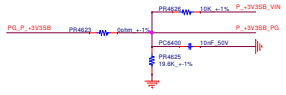
1. VIN
2. EN
3. Output

20250411 Hsinyu
PR4624 change from NI to Stuff



EN High>1.6v,Low<0.4v
EN Abs<6v

PG



MP2145 Pin5, PG internal pull high 500kohm from VIN
Parallel external 10k, Rth=9.8kohm
If Vin = 5V0, insert 19.6kohm for Vpg=3.33V
If Vin = 3V3, No insert 19.6kohm for Vpg =Vin

PG notes
1. Do loading PG
2. Recommend insert 10k, increase sink cability
3. If PG sink cability not enough, please adjust divider resistance

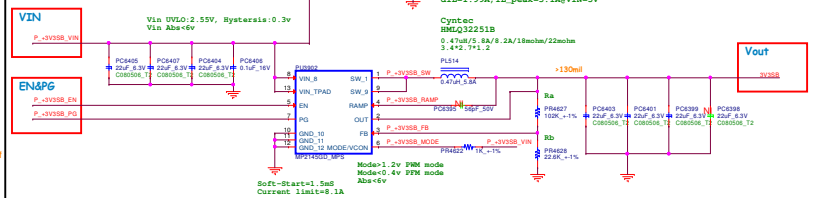
3V3SB(MP2145)

3V3SB Specification:
Vout: 3.3V
Imax: 2.1A
Istep: 1.0A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 1.2MHZ

MP2145
VIN range 2.8~5.5V
Io maximum 6A
QFN 2mm x 3mm
JA=70degC/W

Co-layout : MT3196

All SW/phase/BST net must avoid other net
Especial adjacent layer must GND



Soft-Start=1.5mS
Current limit=8.1A

Mode>1.2v PWM mode
Mode<0.4v PFM mode
Abs<6v

Vout = Vvfb(0.6V) * [1 + (Ra / Rb)]

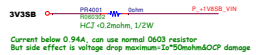
No.	Rail	Ra	Rb	Vout
	0.90V	100k	200k	0.900V
	0.95V	105k	180k	0.950V
	1.00V	100k	150k	1.000V
	1.05V	100k	133k	1.051V
	1.10V	100k	120k	1.100V
	1.15V	110k	120k	1.150V
	1.20V	100k	100k	1.200V
	1.24V	102k	95.3k	1.242V
	1.35V	200k	160k	1.350V
	1.50V	200k	133k	1.502V
	1.70V	187k	102k	1.700V
	1.80V	200k	100k	1.800V
	2.50V	105k	33k	2.509V
	2.56V	52.3k	16k	2.561V
*	3.30V	102k	22.6k	3.308V

Power Source

Input -------->

3.3V

0.603A@Vin=3.3V, eff90.5%,PD=0.189W



Current below 0.94A, can use normal 0603 resistor
But side effect is voltage drop maximum=Io*50mohm&OCP damage

Output <--------

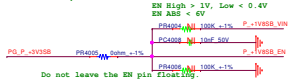
P_+1V8SB

EN

TPSM82823A power sequence

1. VIN
2. EN
3. Output

EN High > 1V, Low < 0.4V
EN ABS < 6V



Do not leave the EN pin float ing.

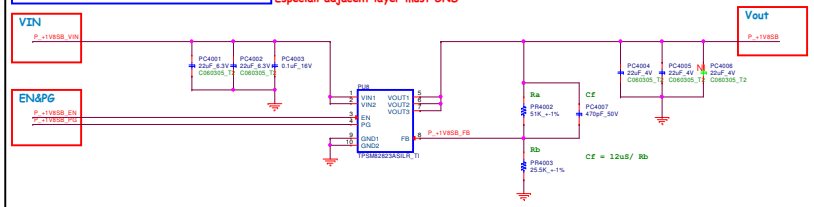
PG

P_+1V8SB (TPSM82823A)

P_+1V8SB Specification:
Vout: 1.8V
Imax: 1.0A
Istep: 0.5A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency: 4MHZ

TPSM82823A
VIN range 2.4~5.5V
Io maximum 3.0A
Frequency = 4MHz
μSiL 2mm x 2.5mm x 1.1m (chock inside)
L=0.24uH
DCR=24mohm(from FAE)
JA=64.3degC/W
Recommend junction < 100degC

All SW/phase/BST net must avoid other net
Especial adjacent layer must GND



Cf = 12uS/ Rb

P2P Table

No.	PN	Vendor	Light Load	Heavy Load
*	TPSM82823A	TI	FCCM	FCCM
	SQ76003D	Silergy	FCCM	FCCM
	MUN3CAD03-JB	Cyntec	FCCM	FCCM

TPSM82821 1A Power save mode
TPSM82821A 1A Forced PWM
TPSM82822 2A Power save mode
TPSM82822A 2A Forced PWM
TPSM82823 3A Power save mode
TPSM82823A 3A Forced PWM

TPSM82823A
Soft-Start=1.25mS
Current limit=3.7~5.0A
Vo= Vfb(0.6V)/Rb *(Ra +Rb)

No.	Rail	Ra	Rb	Vout
	0.90V	12k	24k	0.900V
	0.95V	14k	24k	0.950V
	1.00V	17.4k	26.1k	1.000V
	1.05V	18.7k	24.9k	1.051V
	1.10V	20k	24k	1.100V
	1.15V	22k	24k	1.150V
	1.20V	25.5k	25.5k	1.200V
	1.24V	26.7k	24.9k	1.243V
	1.35V	30k	24k	1.350V
	1.50V	38.3k	25.5k	1.501V
	1.70V	47k	25.5k	1.706V
*	1.80V	51k	25.5k	1.800V
	2.50V	37.4k	11.8k	2.502V
	2.56V	39.2k	12k	2.560V
	3.30V	51k	11.3k	3.308V

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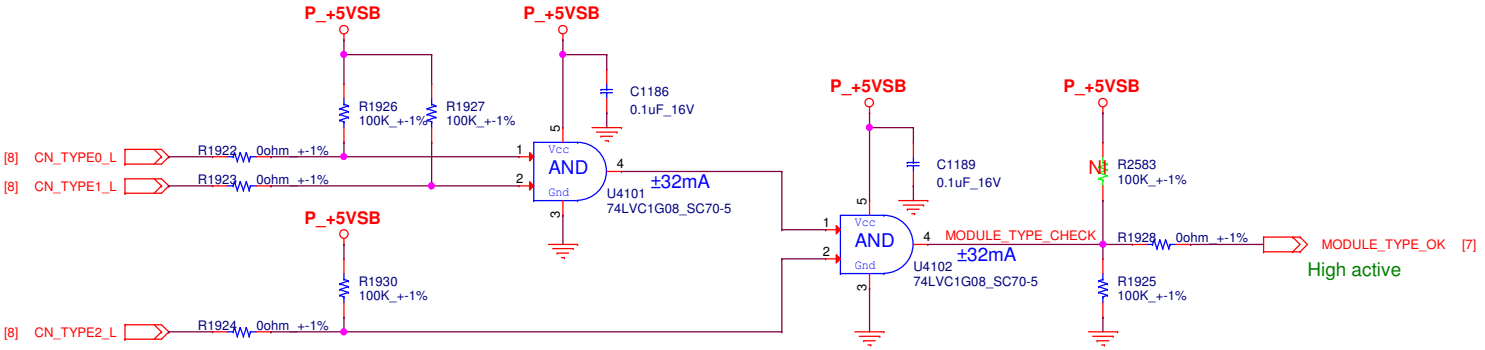
Title: Power_P_+3VSB&P_+1V8SB

Size: D | Document Number: COM-HPC Mini Base | Rev: A1

Date: Wednesday, May 21, 2025 | Sheet 40 of 43

Module Type Dectction

TYPE2	TYPE1	TYPE0	MEANING
NC	NC	NC	Mini Module 8~20V
NC	NC	GND	Reserved
NC	GND	NC	Reserved
NC	GND	GND	Clinet Module 8~20V
GND	NC	NC	Reserved
GND	NC	GND	Reserved
GND	GND	NC	Clinet Module 8~20V
GND	GND	GND	Clinet Module 12V



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Title	Module Type Dectction	
Size: B	Document Number: COM-HPC Mini Base	Rev: A1
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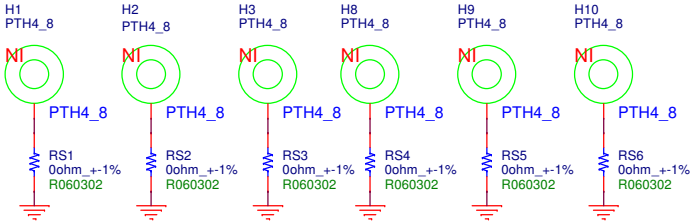
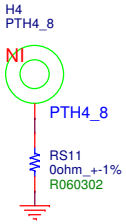
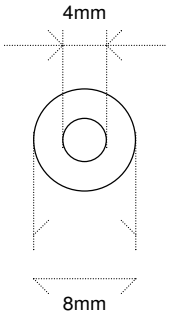
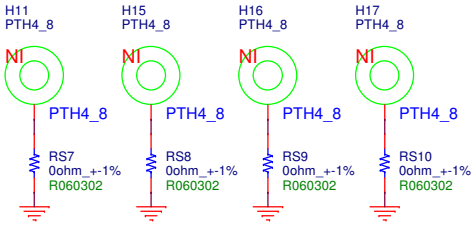
Carrier Board Screw Hole



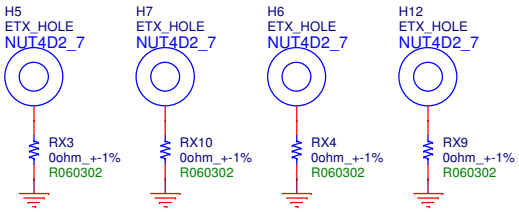


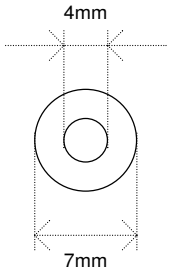




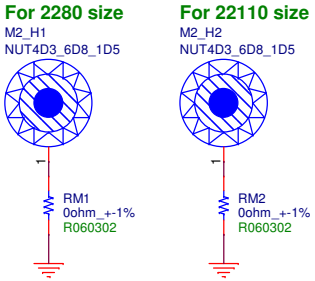
COM-Express Screw Hole

Stand off PN: 33-72186-0100-A0





M.2 sllot Screw Hole



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Title: HOLE		
Size: B	Document Number: COM-HPC Mini Base	Rev: A1
Date: Wednesday, May 21, 2025	Sheet 42 of 43	

Vendor : ADLINK

Part Name : COM-HPC Mini Base board

Item	Date	Page	Change Description	PLM number
A1-1	Apr. 11, 2025	32	Fixed TBT function i. U3201 using FW. change from 72-24256-4610 to 60-77110-F010 ii. U9 using FW. change from 72-02580-1910 to 60-77110-F020 iii. R1018 change from NI to 0 ohm (64-R0005-4510)	DCN-064209
A1-2	Apr. 11, 2025	22	Fixed I2C_0 function i. Remove U75 ii. Stuff R2261 and R2262 (64-R0005-4400)	DCN-064209
A1-3	Apr. 11, 2025	22	Fixed I2C_1 function i. Remove U36 ii. Stuff R904 and R905 (64-R0005-4400)	DCN-064209
A1-4	Apr. 11, 2025	22	Fixed SMB function i. Remove U38 ii. Stuff R906 and R907 (64-R0005-4400)	DCN-064209
A1-5	Apr. 11, 2025	23	Using one power source (VCC_BOOT_SPI) i. Remove R504	DCN-064209
A1-6	Apr. 11, 2025	10	Fixed COM1 function i. Remove R1331 ii. Add R1332. (change from NI to 0 ohm (64-R0005-4400))	DCN-064209
A1-7	Apr. 11, 2025	10	Fixed COM2 function i. Remove R1318 ii. Add R1319. (change from NI to 0 ohm (64-R0005-4400))	DCN-064209
A1-8	Apr. 11, 2025	11	Fixed passive DP dongle i. Add R876. (change from NI to 0 ohm (64-R0005-4400))	DCN-064209
A1-9	Apr. 11, 2025	22	Fixed GSPI function i. Add R1347. (change from NI to 0 ohm (64-R0005-4510))	DCN-064209
A1-10	Apr. 11, 2025	40	Enable 3V3SB i. Add PR4624. (change from NI to 100k (64-10035-4420))	DCN-064209
A1-11	Apr. 11, 2025	11	Enable DP HPD i. Add R50. (change from NI to 0 ohm (64-R0005-4400))	DCN-064209
A1-12	Apr. 11, 2025	12	Enable eDP HPD i. Add R3396. (change from NI to 0 ohm (64-R0005-4400))	DCN-064209
A1-13	Apr. 11, 2025	08, 17	Fixed level shift issue i. U1702 change LSF0204GU12(73-00204-01Z0) to TXS0104ERUTR (73-00104-04Z0) ii. U1847 change LSF0204GU12(73-00204-01Z0) to TXS0104ERUTR (73-00104-04Z0) iii. U1848 change LSF0204GU12(73-00204-01Z0) to TXS0104ERUTR (73-00104-04Z0) iv. U1849 change LSF0204GU12(73-00204-01Z0) to TXS0104ERUTR (73-00104-04Z0) v. U1850 change LSF0204GU12(73-00204-01Z0) to TXS0104ERUTR (73-00104-04Z0) vi. U1853 change LSF0204GU12(73-00204-01Z0) to TXS0104ERUTR (73-00104-04Z0)	DCN-064209
A1-14	Apr. 22, 2025	17	Fixed Front panel audio connector issue Remove F_AUD (21-6110E-2050)	DCN-064307
A1-15	Apr. 22, 2025	16	Remove unless SIO switch jump pin i. Remove JP43 (21-6110E-1030) ii. Remove JP43_1 (25-10051-1020)	DCN-064307
A1-16	Apr. 22, 2025	08	Fix P_+1V8 leakage voltage i. Remove R1213 (64-10025-4410) ii. Remove R1215 (64-10025-4410)	DCN-064307
A1-17	May. 20, 2025	22	Fix P_+1V8SB leakage voltage i. Remove R834 (64-10015-4490) ii. Remove R835 (64-10015-4490) iii. Remove R1344 (64-10015-4490) iv. Remove R1345 (64-10015-4490) v. Remove R836 (64-10015-4490) vi. Remove R837 (64-10015-4490)	DCN-064611
A1-18	May. 20, 2025	07	Enable wide range input design i. Remove R911 (64-R0005-4400) ii. Add R596 (change from NI to 4.7k (64-47015-4490))	DCN-064611
A1-20	May. 20, 2025	16	Remove buzzer support i. Remove BUZZER1 (23-50005-0000) ii R495 change from 2.2k (64-22015-4520) to 33 ohm (64-33R05-3550) iii. Add R496 (change from NI to 4.7k (64-47015-4490))	DCN-064611
A1-21	May. 28, 2025	08, 18, 20	Modify the PCIE CLK topology. (Using CLK Buffer as source to the PCIE device, reserved the REFCLK IN pin of ROW ABCD for future design) i. Remove 0 ohm (64-R0005-4400) (R3381, R3378, R3379, R3374, R3371, R3372, R3412, R3413, R3380, R3410, R3411) ii Add 0 ohm (64-R0005-4400) (R3382, R1224, R1223, R3375, R1190, R1191, R1153, R1152)	DCN-064698

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Title: Change_History

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Date: Friday, June 20, 2025 | Sheet 43 of 43