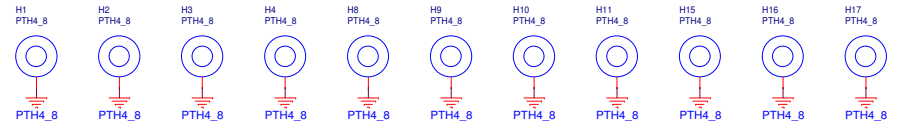


Express-BASE6 R3.1 Rev.A1

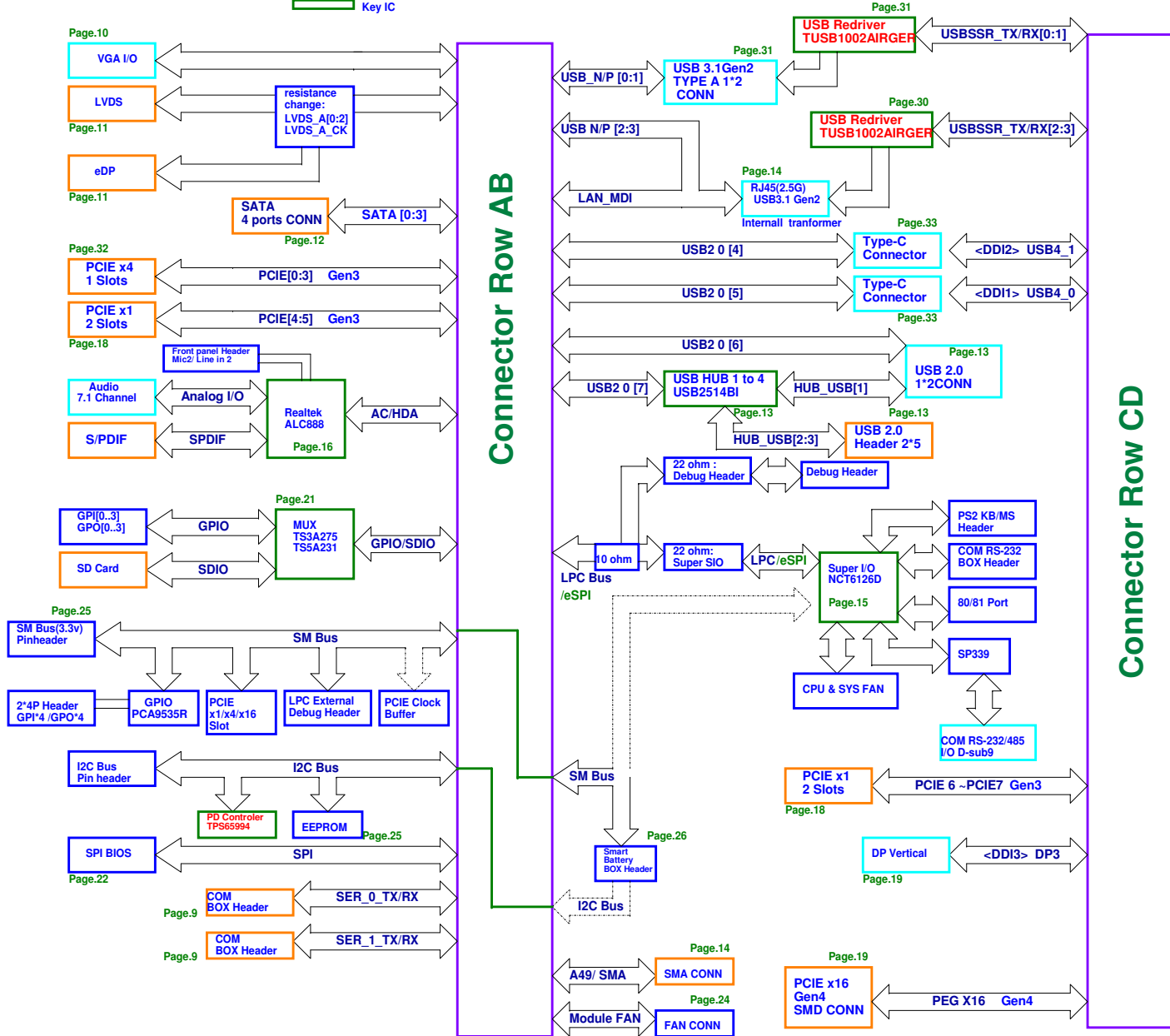
COM-Express Base Board
PICMG COM.0 Rev 3.1

PCB Size : 304.8 mm x 243.84 mm
(12000mils x 9600mils)

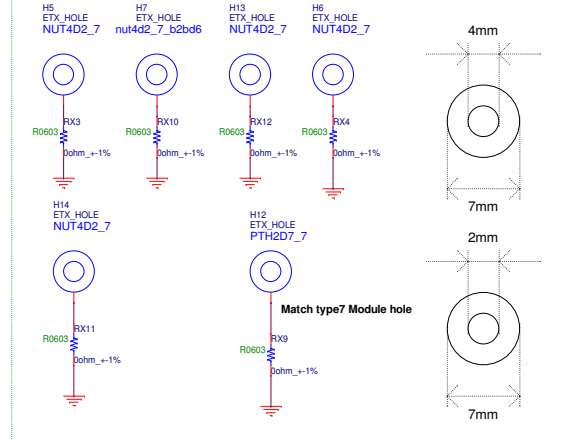
ADLINK P/N : 77107-0A10-A0



Block Diagram



COM-Express Screw Hole



Page

| | | | |
|----|------------------------------|----|----------------------------|
| 01 | Cover Page & BLOCK Diagrams | 29 | Reserved |
| 02 | Power Distribution | 30 | USB3.0_Rear I/O |
| 03 | SMBUS/I2C/CLK Distribution | 31 | USB3.0_Gen2_1*2 |
| 04 | Power design(Power ON)&REST | 32 | PCI EXPRESS x4 |
| 05 | Power design(Power Off) | 33 | PD_TPS65994E_Type-C |
| 06 | Power design(S3) | 34 | Burnside Bridge_POWER/GND |
| 07 | Power | 35 | Burnside Bridge_MISC_DEBUG |
| 08 | COM Express Connector | 36 | Burnside Bridge_TBT Port |
| 09 | Module series port | 37 | Change History |
| 10 | VGA | | |
| 11 | Panel & Backlight Power&LVDS | | |
| 12 | SATA | | |
| 13 | USB 2.0 & USB2.0 HUB | | |
| 14 | Giga LAN_2.5G&USB3.1 Gen2 | | |
| 15 | SIO_NCT6126D | | |
| 16 | Audio_1_Audio_1_ALC888 | | |
| 17 | Audio_2 | | |
| 18 | PCI EXPRESS x 1 | | |
| 19 | PCI EXPRESS x 16 & DP DDI3 | | |
| 20 | Clock Buffer | | |
| 21 | Misc. & GPIOs & SD CARD | | |
| 22 | External BIOS& SPI connector | | |
| 23 | LPC Debug Module | | |
| 24 | Module FAN & PCA9535 | | |
| 25 | I2C Eeprom,LPC | | |
| 26 | TPM&Smart Battery | | |
| 27 | eDP | | |
| 28 | Power(5VSB to 3VSB)&1V8SB | | |

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Cover Page & BLOCK Diagrams
 Size C Document Number Express-BASE6 R3.1 Rev A1
 Date: Saturday, December 03, 2022 Sheet 1 of 38

ATX Power Supply
4 pin 12V connector

COM Express Module

ROW CD Connector

VCC_12V @6A

ROW AB Connector

VCC_12V @6A
VCC_5V_SBY @2A

ATX Power Supply
24 pin connector

Thermaltake
Smart BM2 550W

54A
PSU_12V

PSU_5V
20A

PSU_3V3
20A

2.5A
5VSB

5VSB

5VCC_SB_MOD

P12V_4P

P12V_4P

MPM3833C

PWM
MP2145GD

MPM3833C

P3V3

0 ohm /0603

PW_P3V3_S0

0 ohm /0603

3V3SB

0 ohm /0603

PW_P3V3_S0

0 ohm /0603

PW_P3V3_SX

RETIMER_PD_PWR_EN_R
From PD-TPS65994B_GPIO0 Control

load Switch
EN high

BB_3V3_SX

P12V

PCIEX1 *4

2.1A => 8.4A

P3V3

3A => 12A

3V3SB

0.375A => 1.5A

P12V

PCIEX16 *1

5.5A

P3V3

3A

3V3SB

0.375A

P3V3

ALC888

5VSB

0.01A

0.04A

P3V3

SPI Flash

0.03A

P3V3

USB redriver *4

0.1A => 0.4A

P3V3

Panel LVDS

0.96A

P12V

SATA power *1

0.6A

P5V

1.44A

P12V

FAN *3

1A => 3A

P5V

USB2.0 *6

0.5A => 3A

P5V

USB3.1 GEN2 *4

0.9A => 3.6A

P5V

DP I/O *1

0.5A

P3V3

NCT6126_SIO

0.02A

0.01A

JP39

1V8SB

3V3SB

BB_3V3_SX

Intel Burnside Bridge*2

500mA

P3V3

100MHz/ 2A G Bead

3V3SB

100MHz/ 2A G Bead

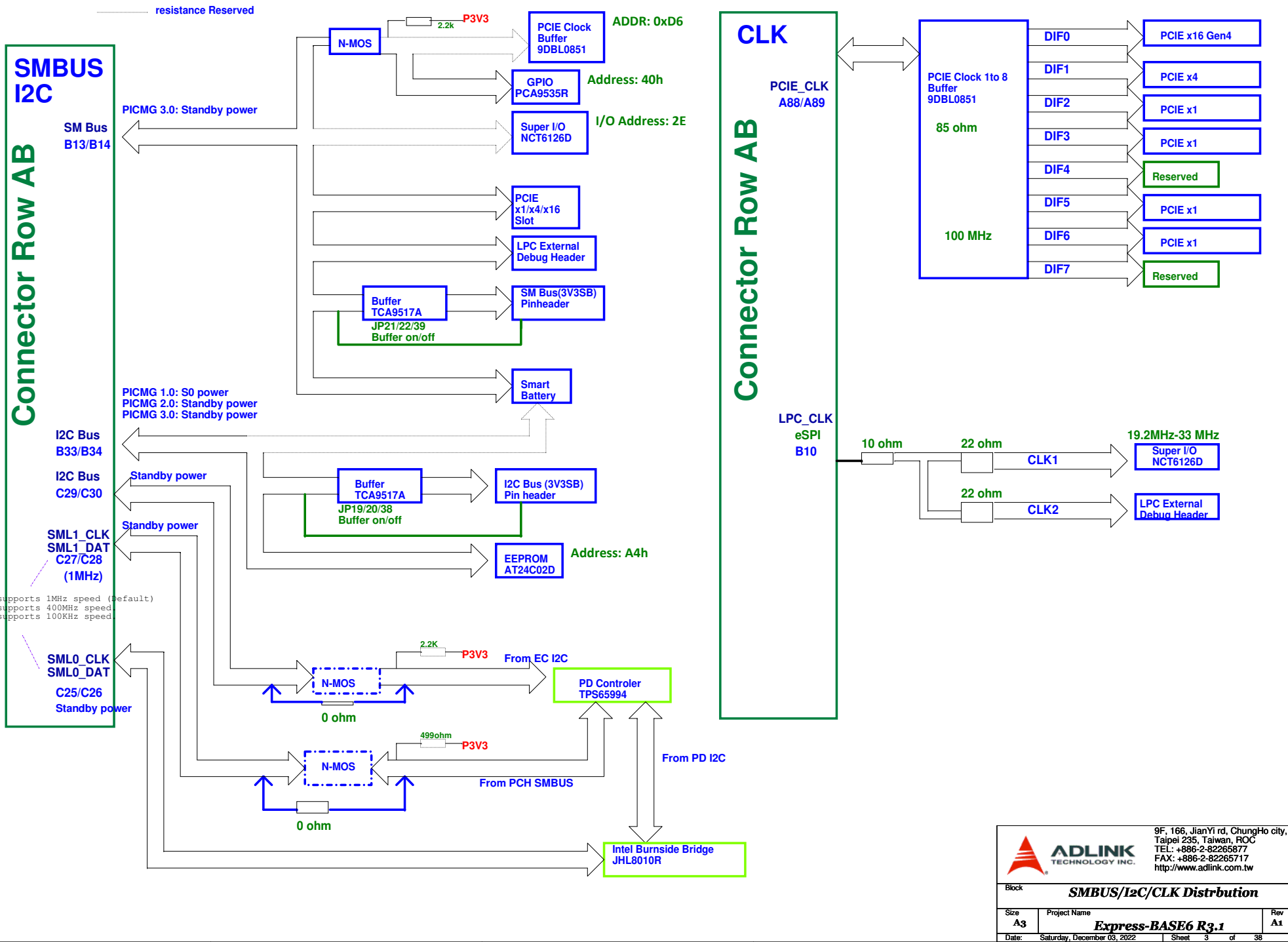
PD Controller TPS65994

0.003A



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| | | |
|-------|-----------------------------|---------------|
| Block | Power Distribution | |
| Size | Project Name | Rev |
| C | Express-BASE6 R3.1 | A1 |
| Date: | Saturday, December 05, 2022 | Sheet 2 of 38 |



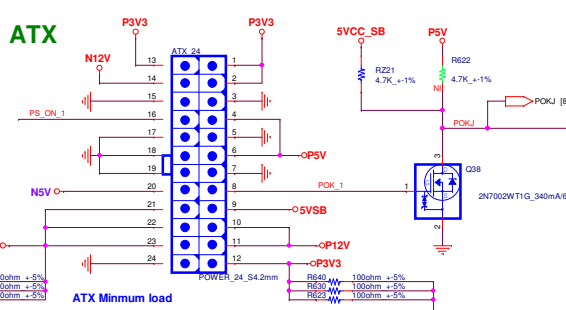
499ohm supports 1MHz speed (default)
 2.2Kohm supports 400MHz speed
 10Kohm supports 100KHz speed

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| | | |
|-------|-----------------------------------|---------------|
| Block | SMBUS/I2C/CLK Distribution | |
| Size | Project Name | Rev |
| A3 | Express-BASE6 R3.1 | A1 |
| Date: | Saturday, December 03, 2022 | Sheet 3 of 38 |

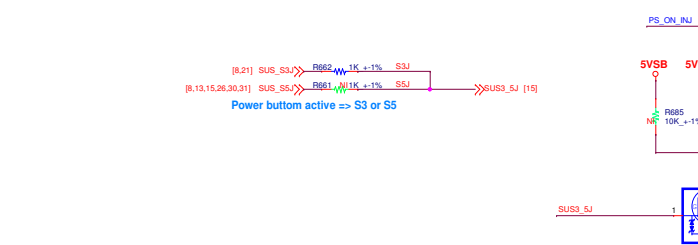
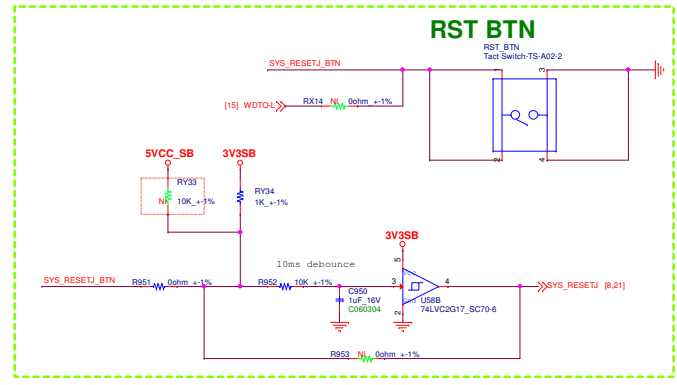
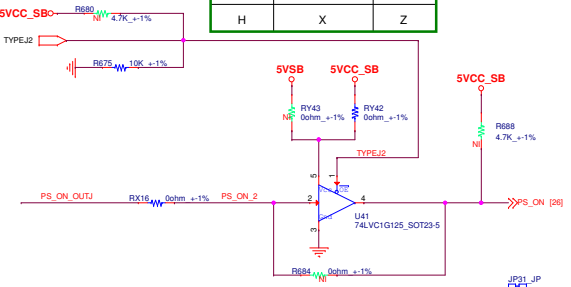
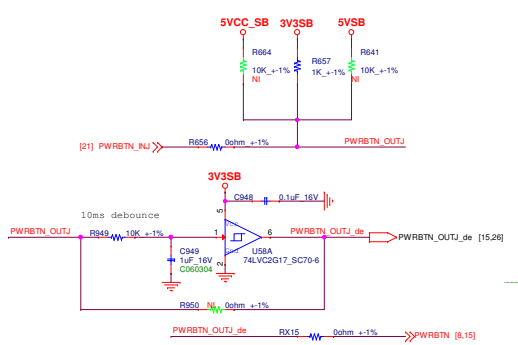
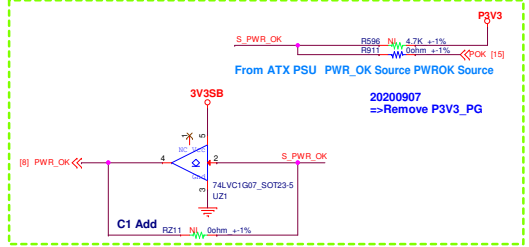
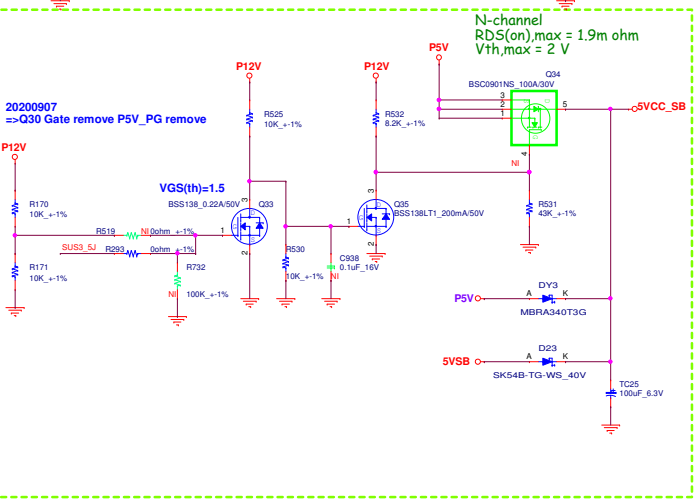
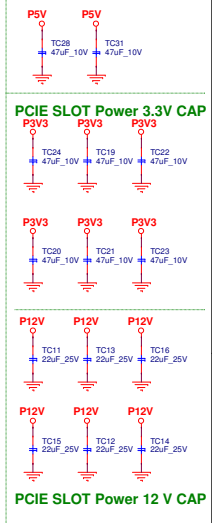
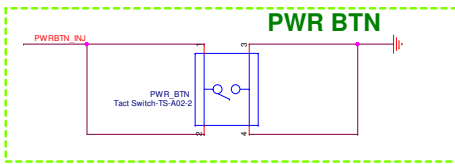
ATX



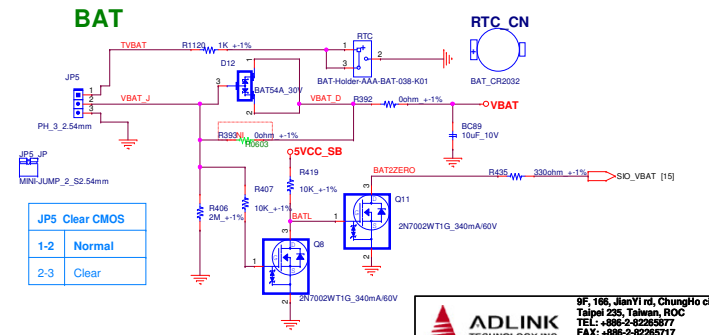
20200902 P3V3 to P1V5
=>Remove codec power 1.5V

LDO 20200921 5VCC_SB to 3V3SB
=>Remove LDO 3.3VSB

PWR BTN



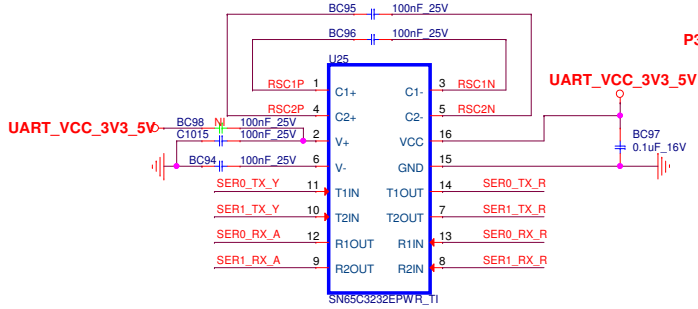
BAT



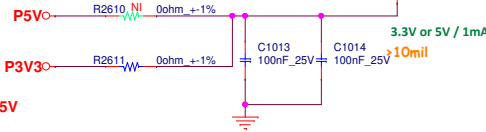
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RS232 from module

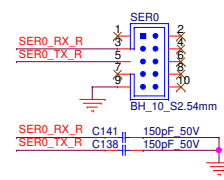
TYPE 6
Add RS232



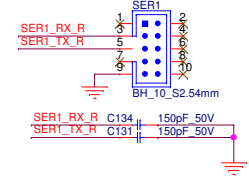
UART_VCC_3V3_5V



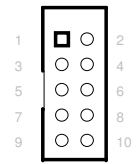
Port 0



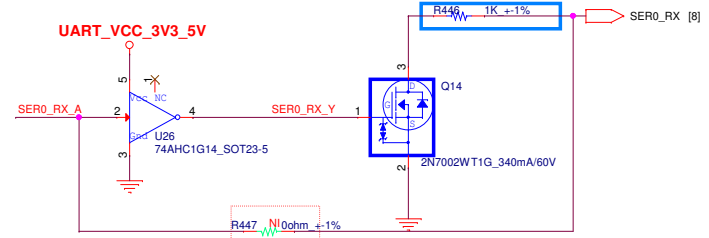
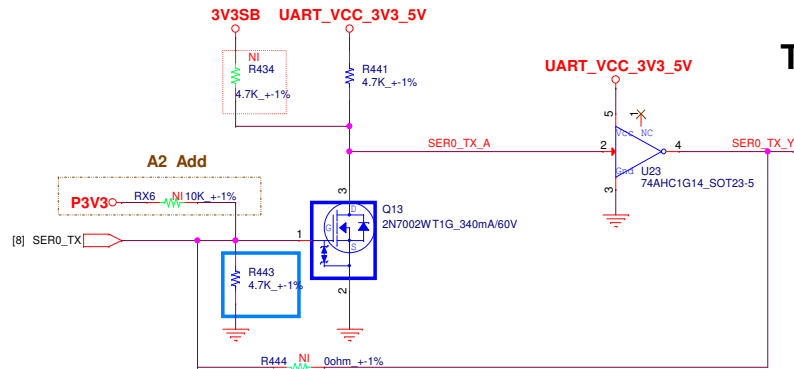
Port 1



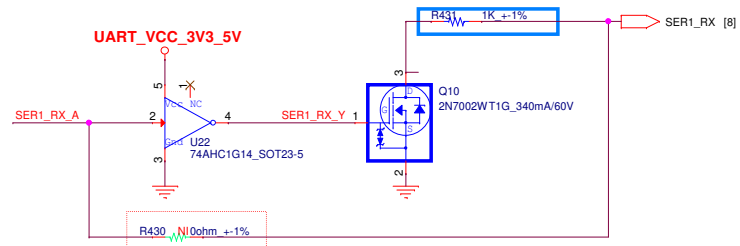
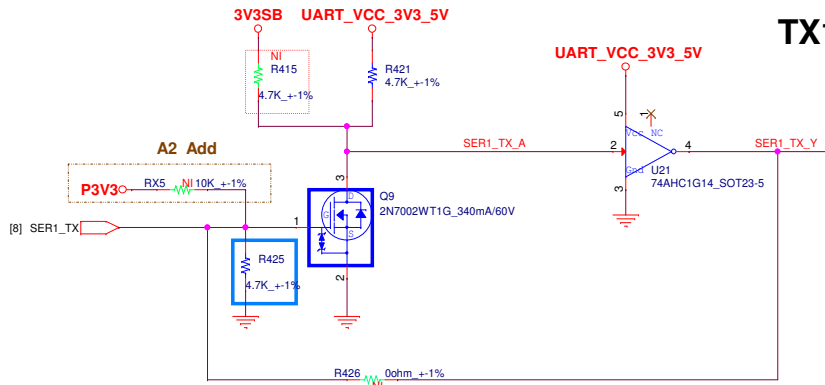
74-00339-0FR0 => SP339



TX0 / RX0



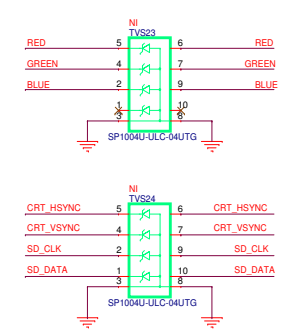
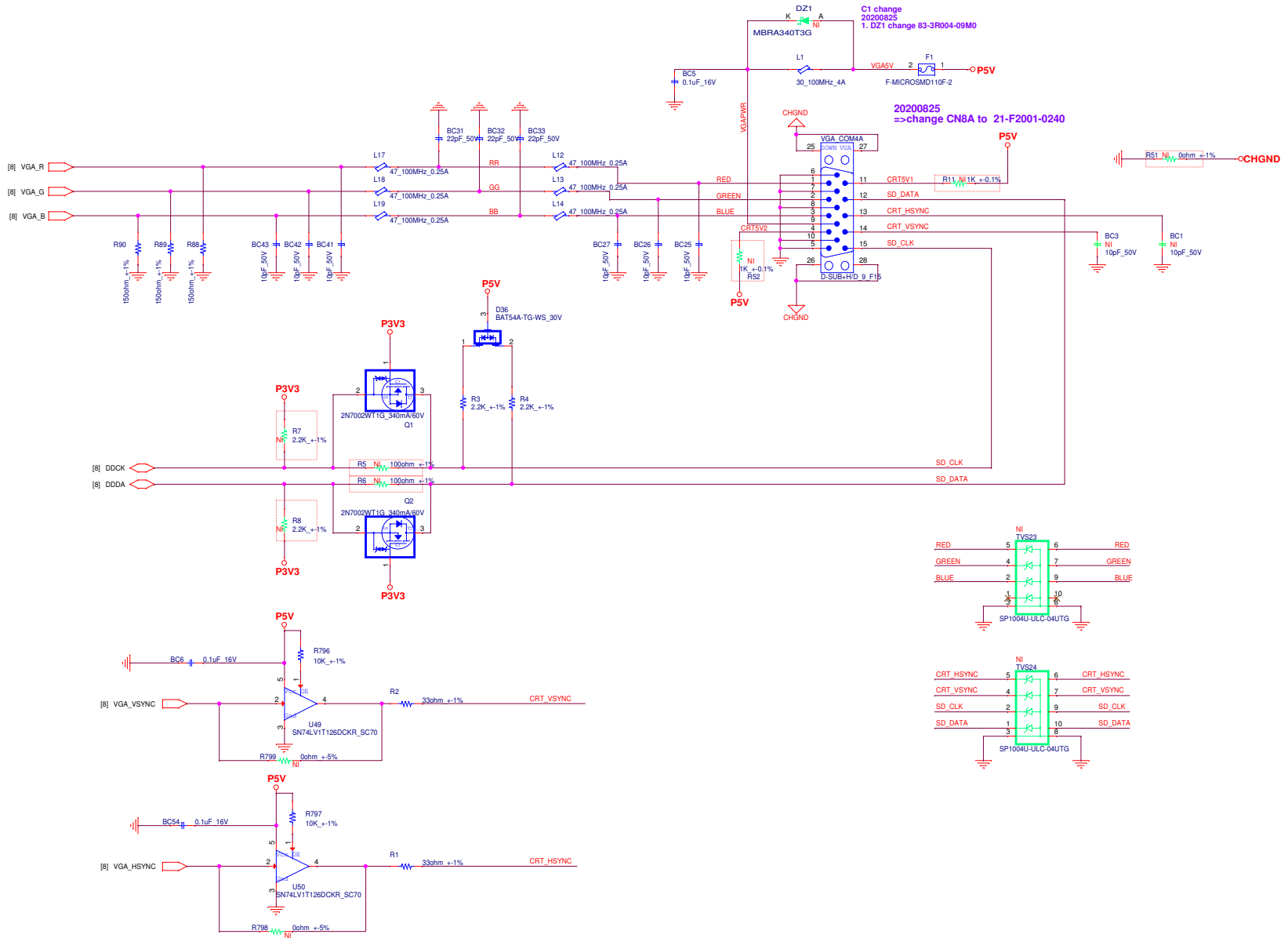
TX1 / RX1



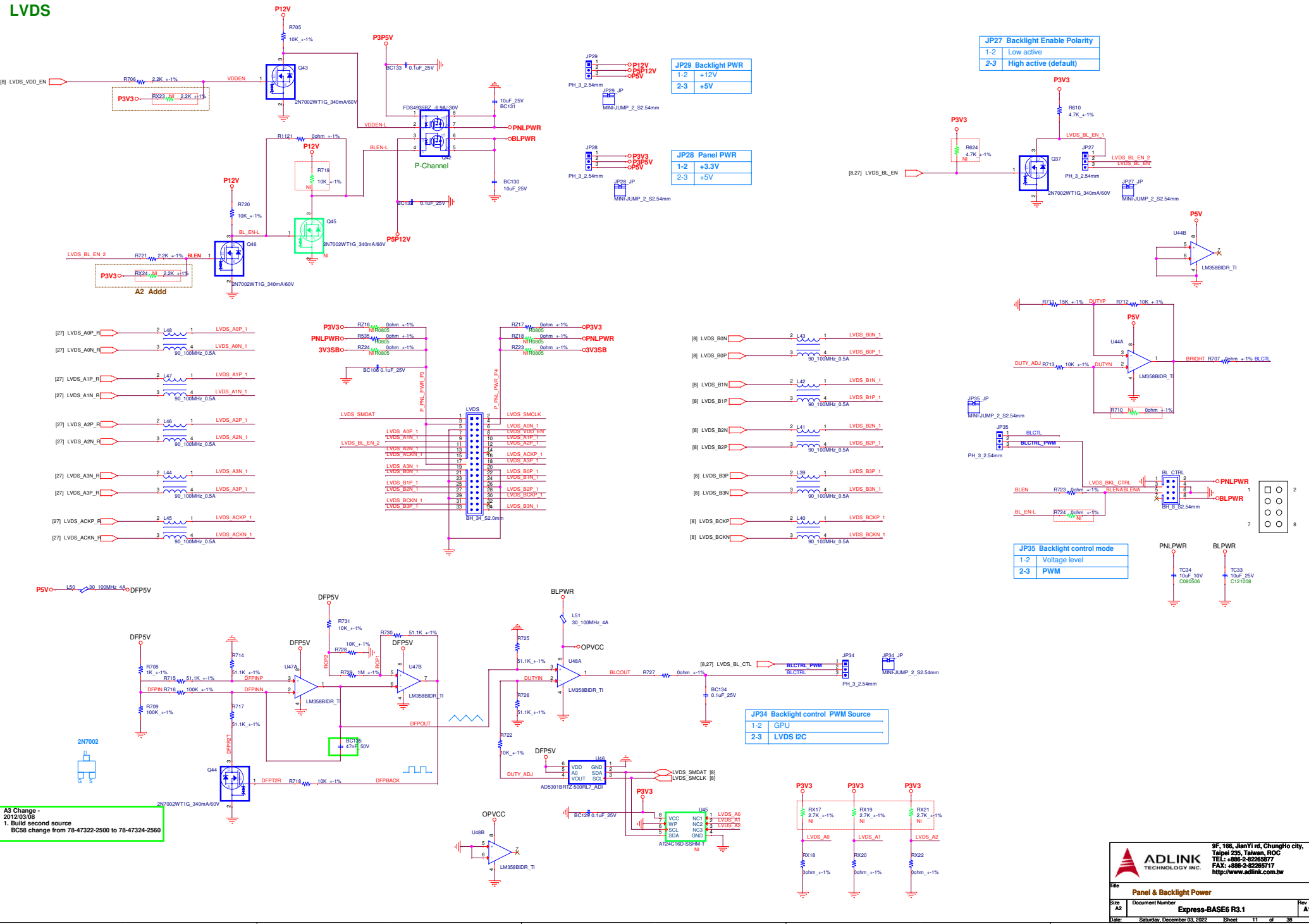
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| | | | |
|-------|-----------------------------|--------------------|--------------------|
| Title | | | Module series port |
| Size | Document Number | Express-BASE6 R3.1 | |
| A3 | | | Rev A1 |
| Date: | Saturday, December 03, 2022 | Sheet | 9 of 38 |

VGA



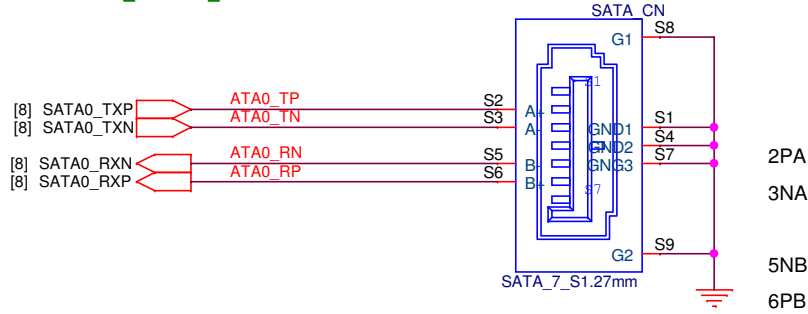
LVDS



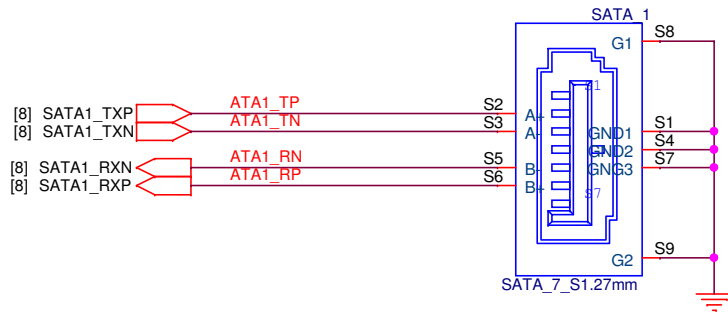
A3 Change - 2012/03/08
1. Build second source
BC58 change from 78-47322-2500 to 78-47324-2560

SATA [0:3]

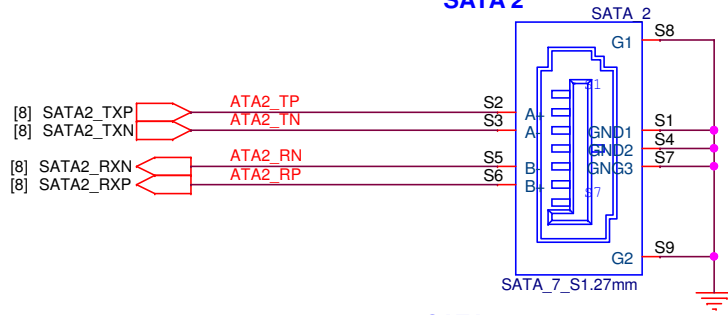
SATA 0



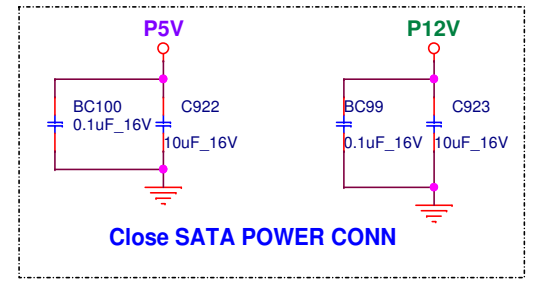
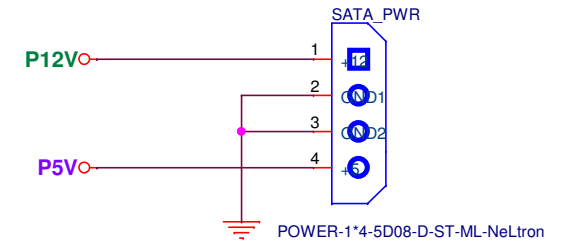
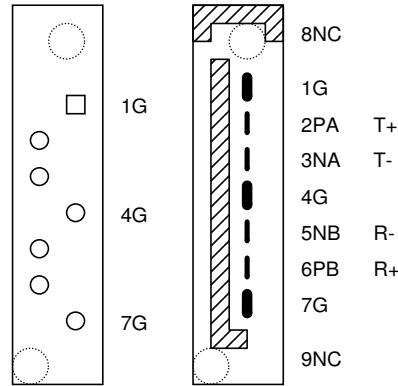
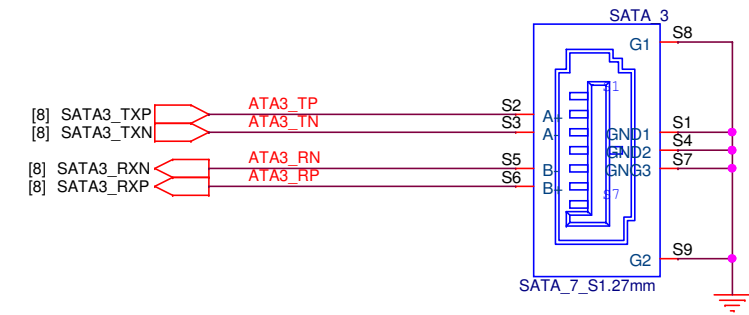
SATA 1



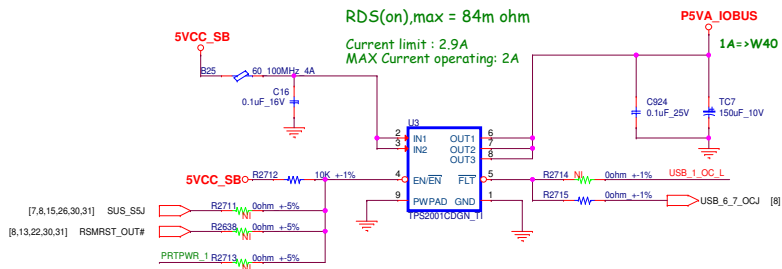
SATA 2



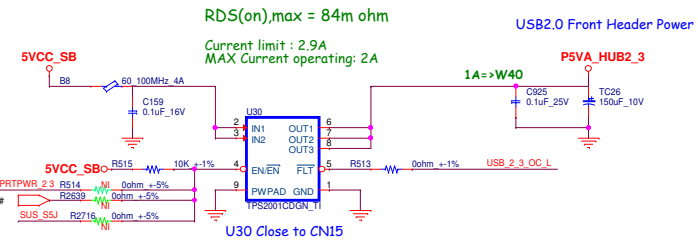
SATA 3



| | | | |
|-----------------------------------|--|--|-----------|
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| | | Title SATA | |
| Size A4 | Document Number Express-BASE6 R3.1 | | Rev A1 |
| Date: Saturday, December 03, 2022 | | Sheet 12 of 38 | |

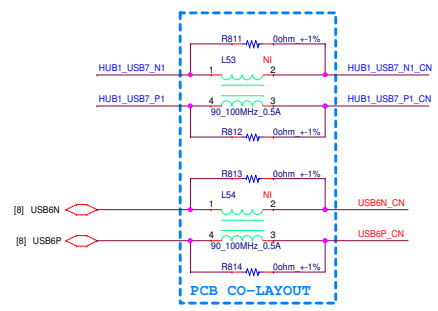


RDS(on),max = 84m ohm
 Current limit : 2.9A
 MAX Current operating: 2A

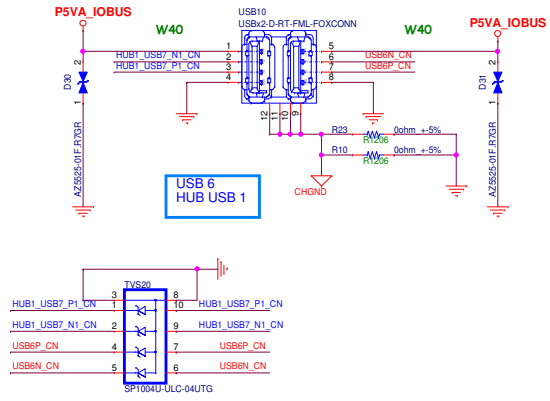


RDS(on),max = 84m ohm
 Current limit : 2.9A
 MAX Current operating: 2A

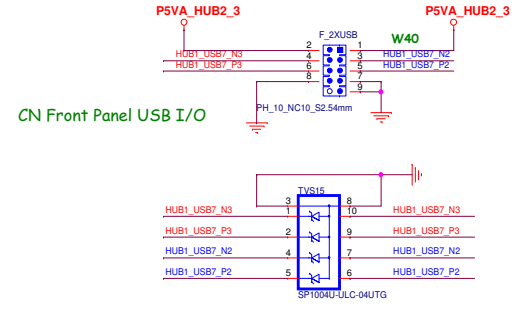
USB2.0 Front Header Power



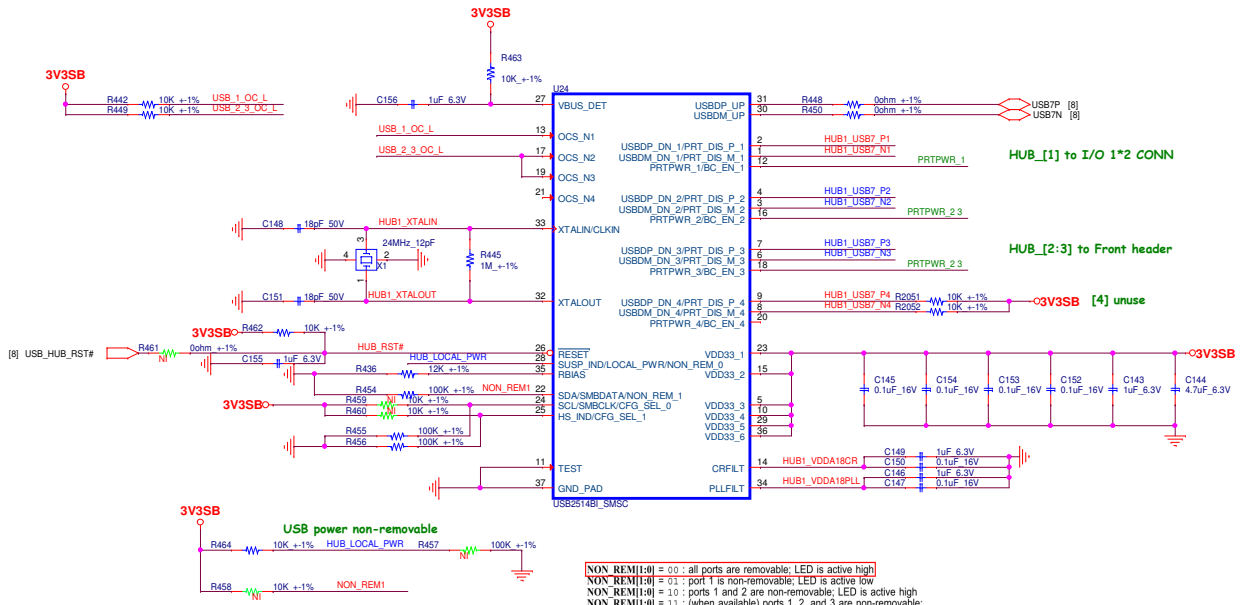
PCB CO-LAYOUT



USB 6 HUB USB 1



CN Front Panel USB I/O



NON_REM1[0] = 00 : all ports are removable; LED is active high
 NON_REM1[0] = 01 : port 1 is non-removable; LED is active low
 NON_REM1[0] = 10 : ports 1 and 2 are non-removable; LED is active high
 NON_REM1[0] = 11 : (when available) ports 1, 2, and 3 are non-removable; LED is active low

Table 5.1 Initial Interface/Configuration Options

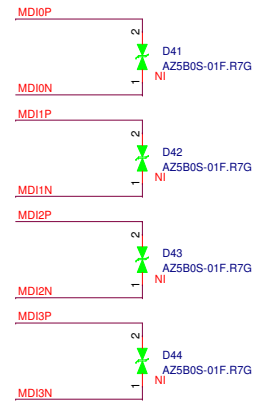
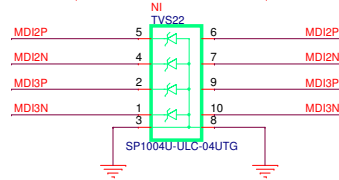
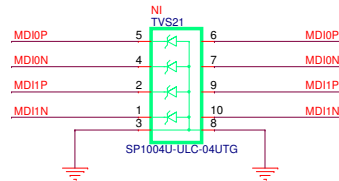
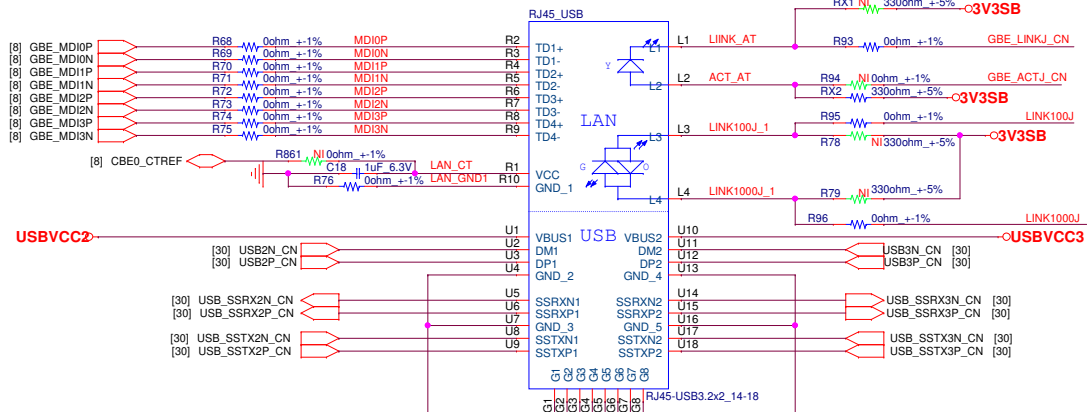
| CFG_SEL[1] | CFG_SEL[0] | DESCRIPTION |
|------------|------------|--|
| 0 | 0 | Default configuration: • Strap options enabled • Self-powered operation enabled • Individual power switching • Individual over-current sensing |
| 0 | 1 | The hub is configured externally over SMBus (as an SMBus slave device) • Strap options disabled • All registers configured over SMBus |
| 1 | 0 | Default configuration with the following overrides: • Bus-powered operation |
| 1 | 1 | The hub is configured over 2-wire I ² C EEPROM: • Strap options disabled • All registers configured by I ² C EEPROM |



Giga LAN (2.5G)_RJ45+USB3.1 Gen2

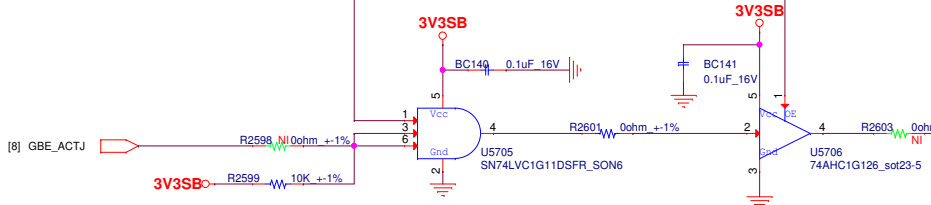
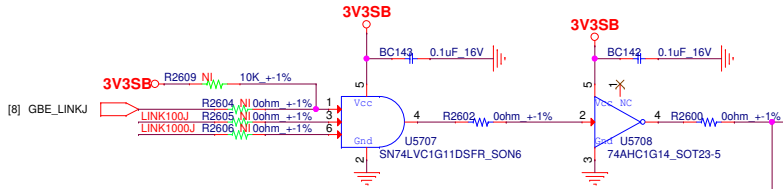
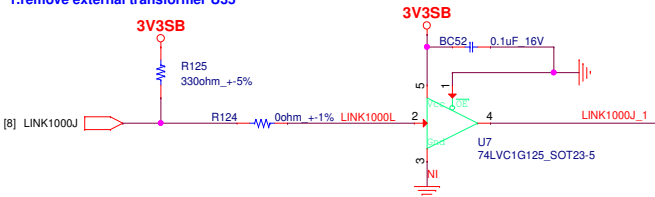
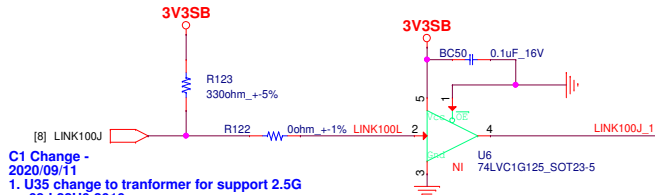
Type 6
Modify

USB[2:3]



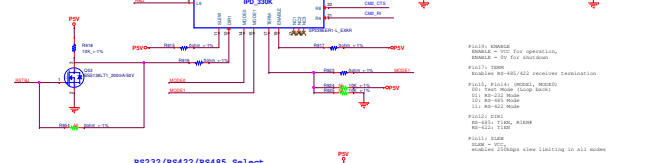
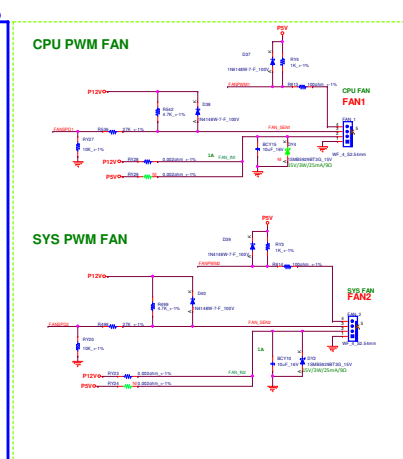
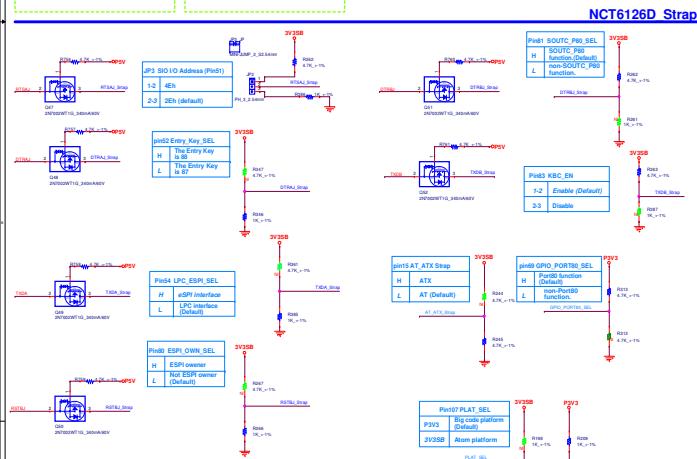
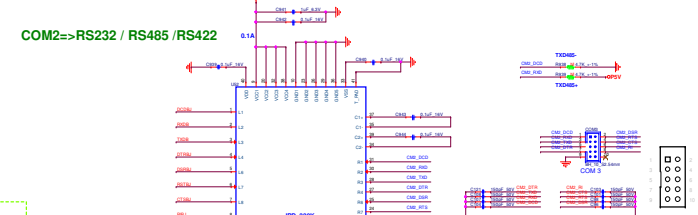
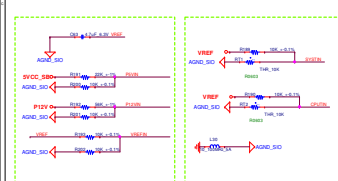
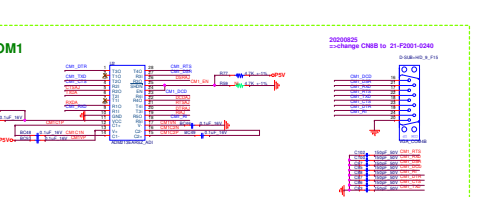
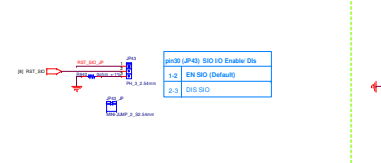
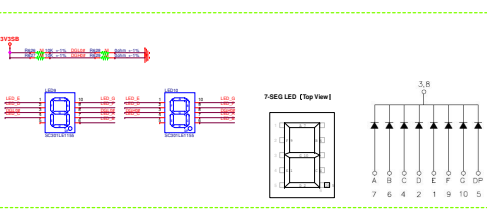
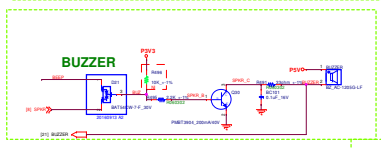
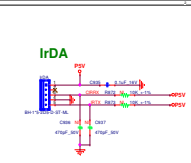
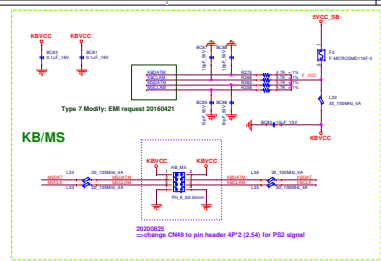
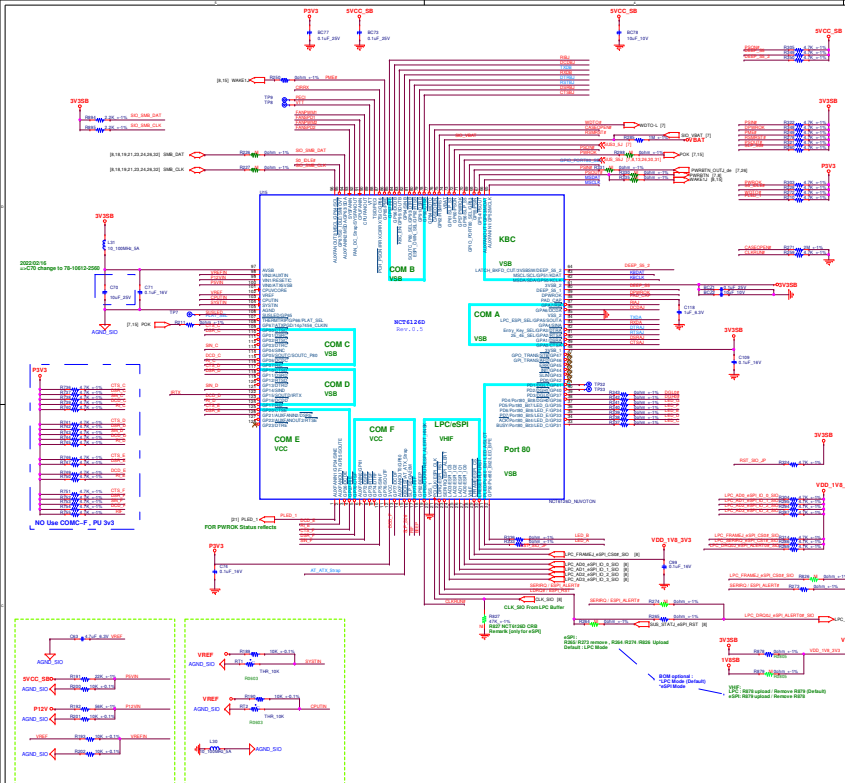
| Emitting Color | λp (nm) | Vf @If=20mA | Ir @Vf=5V |
|----------------|---------|-------------|-----------|
| Green | 570 | 1.7 ~2.6 V | 10μA max. |
| Orange | 605 | 1.7 ~2.6 V | 10μA max. |
| Yellow | 588 | 1.7 ~2.6 V | 10μA max. |

C1 Change -
2020/09/11
1. U35 change to transformer for support 2.5G
=> 68-L22H0-3010
2020/09/28
1.remove external transformer U35



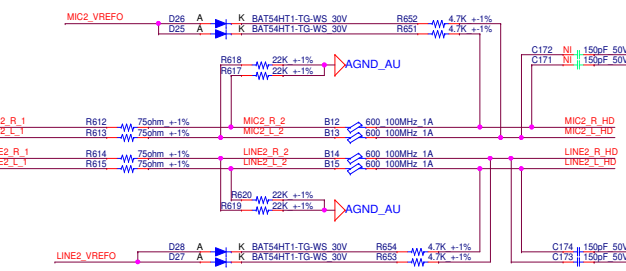
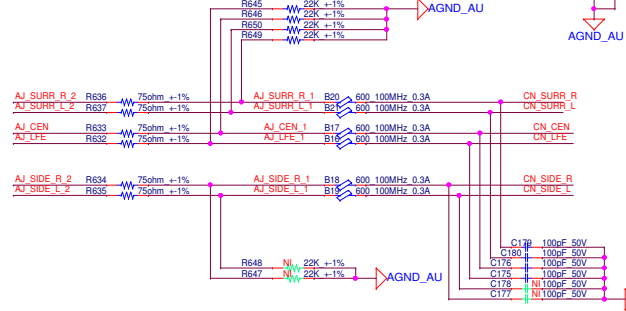
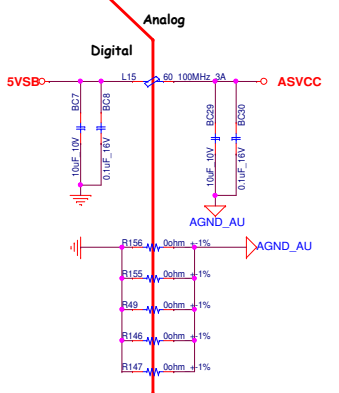
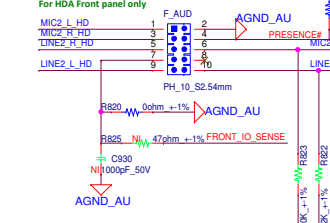
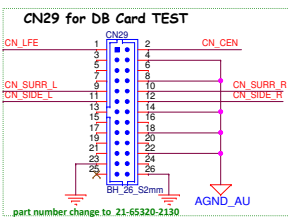
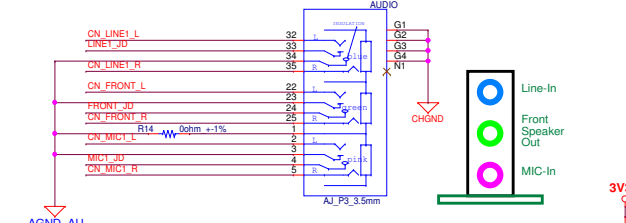
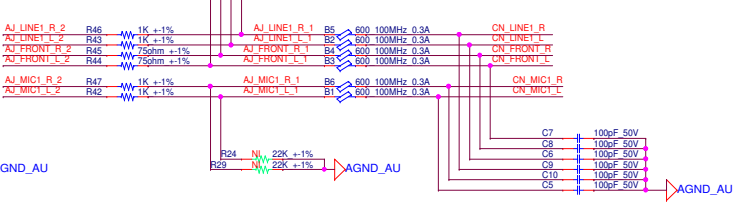
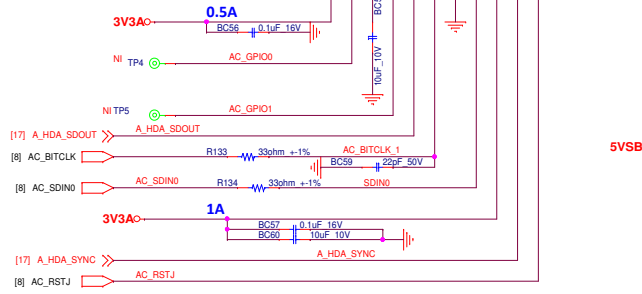
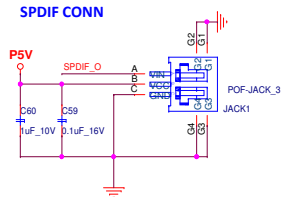
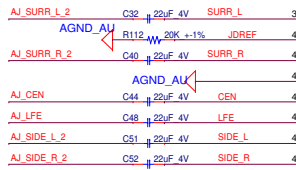
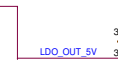
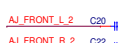
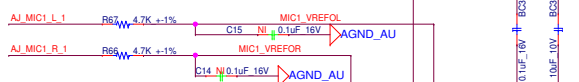
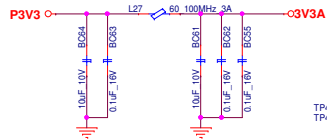
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| | | | |
|---|--|-------|------------------|
| Title Giga LAN 2.5G&USB3.1 Gen2 | | | Rev A1 |
| Size A3 | Document Number Express-BASE6 R3.1 | | |
| Date: Saturday, December 03, 2022 | Sheet 14 | of 38 | |



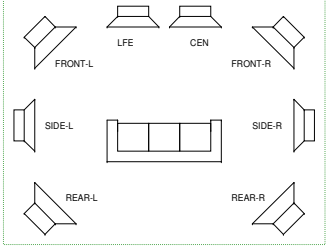
RS232/RS422/RS485 Select

| | MODE1 | MODE0 |
|--------|-------|-------|
| RS-232 | 0 | 1 |
| RS-485 | 1 | 0 |
| RS-422 | 1 | 1 |



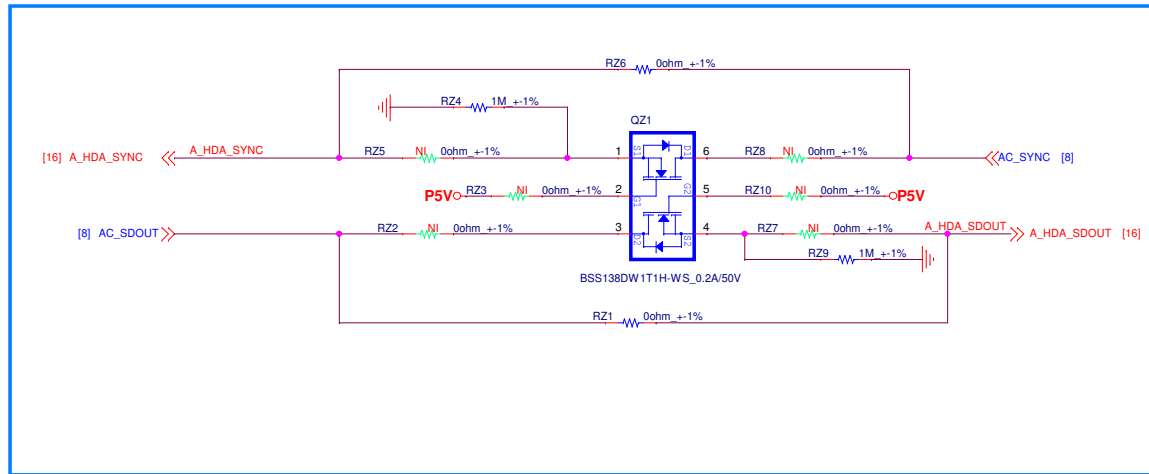
Configuration 1: (7.1 Channel Solution)
 Rear Panel: 6 jacks have specific functionality
 Front Panel: 2 or 3 jacks are Universal Audio Jack

| Pin Assignment | Location | Re-tasking |
|----------------------|-------------|------------------------------------|
| FRONT (pin-35/36) | Back Panel | AMP output, line input |
| SURR (pin-39/41) | Back Panel | Line output, line input |
| CEN/LFE (pin-43/44) | Back Panel | Line output, line input |
| SIDESURR (pin-45/46) | Back Panel | Line output, line input |
| LINE1 (pin-23/24) | Back Panel | Line output, line input |
| MIC1 (pin-21/22) | Back Panel | Line output, line input, mic input |
| LINE2 (pin-14/15) | Front Panel | AMP output, line input, mic input |
| MIC2 (pin-16/17) | Front Panel | AMP output, line input, mic input |



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| | | |
|------|-----------------|--------------------|
| File | | Audio_1_ALC888 |
| Size | Document Number | Express-BASE6 R3.1 |
| Date | Sheet | 16 of 38 |



B1 Change -
 2012/12/26
 The S3 power leakage problem occurs when pull-up strapping resistors are used at the HD Audio bus SYNC or SDO line

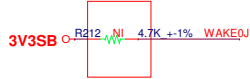
1. QZ1 Add 84-00138-03E0
2. RZ20,RZ19,RZ17,RZ21 Add 0 ohm(63-R0003-4410)(0402)
3. RZ11,RZ18 Add 1M ohm(64-10045-4490)(0402)

2013/01/08

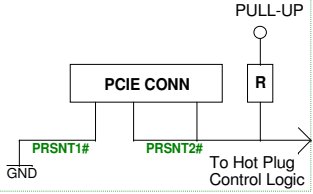
1. CN27 Change from 20-92001-0050 to 20-92090-0050 (20-92090-0050 footprint: dcnn_techbest_dlt1160a-g)

| | | | |
|--------------------------------------|--|--|----------|
| | | 9F, 166, JianYi rd, ChungHo city, Taipei 235, Taiwan, ROC TEL.: +886-2-82265877 FAX: +886-2-82265717 http://www.adlink.com.tw | |
| | | Title Audio_2 | |
| Size A3 | Document Number Express-BASE6 R3.1 | Rev A1 | |
| Date: Saturday, December 03, 2022 | Sheet 17 | | of 38 |

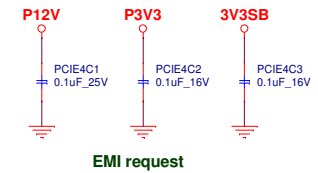
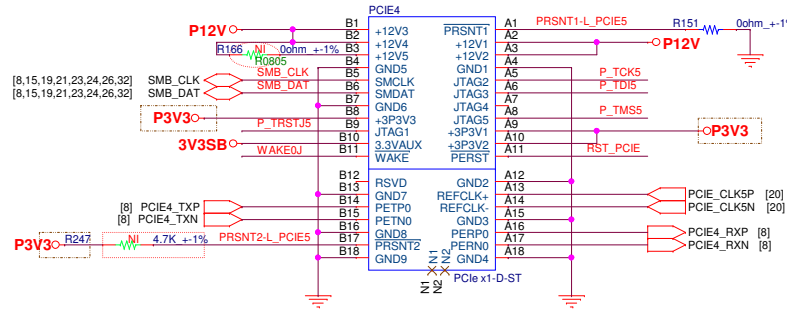
The WAKE# signal is an open drain, active low signal that is driven low by a PCI Express component to reactivate the PCI Express slot's main power rails and reference clocks.



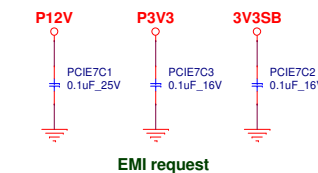
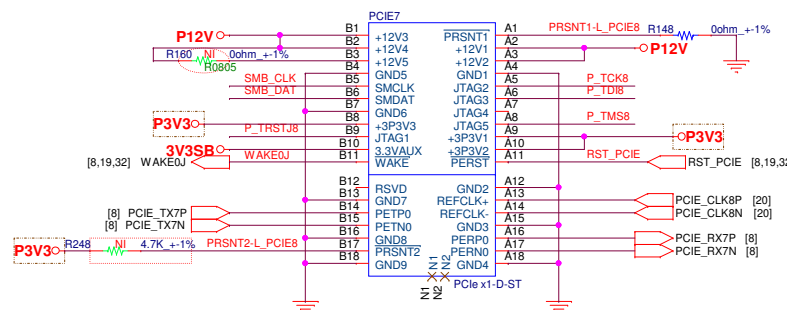
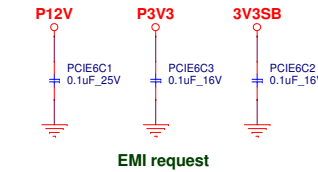
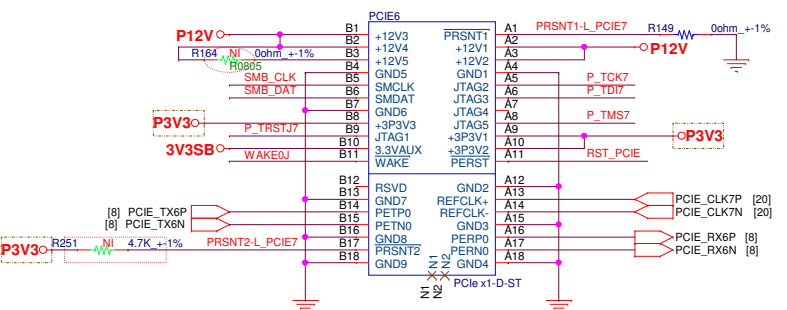
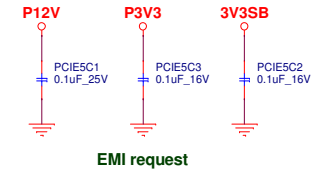
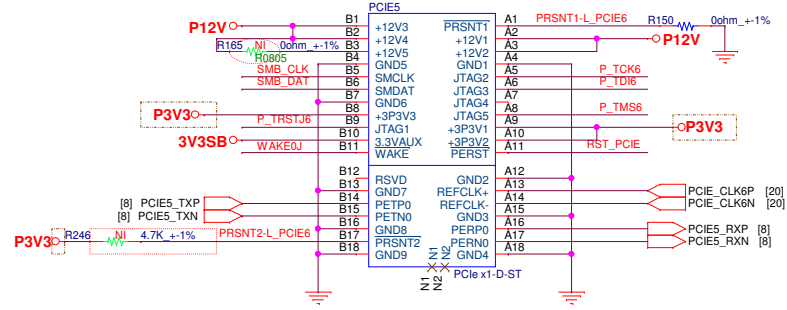
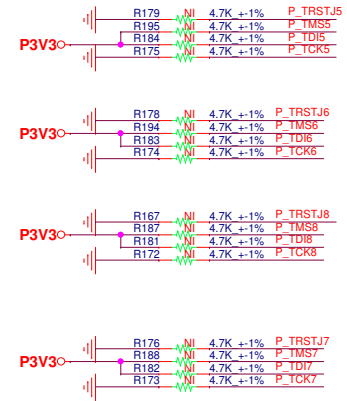
PCI Express Hot-Plug controller detects



**PCIE X1
SMT SLOT: 61-L1000-0360
DIP SLOT: 21-51511-0360**

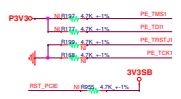
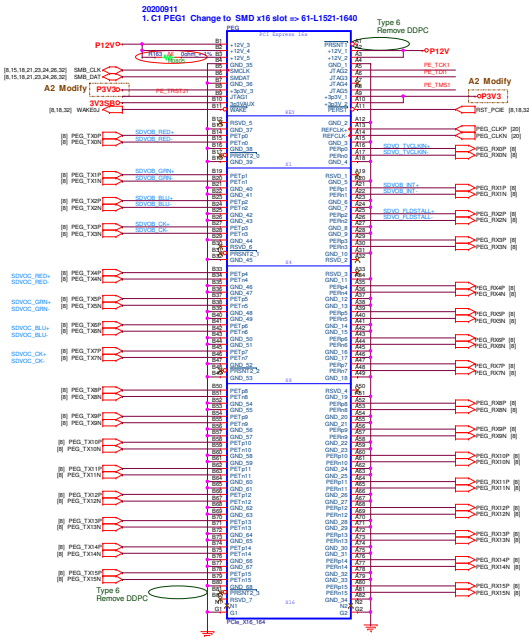


A2 Modify

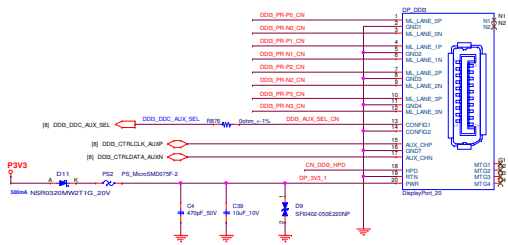


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| | | | |
|--------|-----------------------------|--------------------|----------|
| File | | PCI EXPRESS x 1 | |
| Size | Document Number | Express-BASE6 R3.1 | |
| Custom | | | Rev A1 |
| Date: | Saturday, December 03, 2022 | Sheet | 18 of 38 |



DP Vertical Connector / DDI3



Power Supply Rail Requirements

| Power Rail | x1 Connector | x16 Connector |
|--------------------|--------------|---------------|
| +3.3V | | |
| Voltage tolerance | 9% | 9% |
| Supply Current | 3.0 A | 3.0 A |
| Capacitive Load | 1000 uF | 1000 uF |
| +12V | | |
| Voltage tolerance | 8% | 8% |
| Supply Current | 0.5 A | 4.4 A |
| Capacitive Load | 300 uF | 2000 uF |
| +3.3Vaux | | |
| Voltage tolerance | 9% | 9% |
| Supply Current | 375 mA | 375 mA |
| Wake-up Enabled | 20 mA | 20 mA |
| Non-wakeup Enabled | 150 uF | 150 uF |
| Capacitive Load | 25 W | 60 W |

The power supply rails available at the PCI Express connectors, based on the number of PCI Express lanes supported by the connectors.

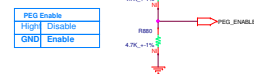
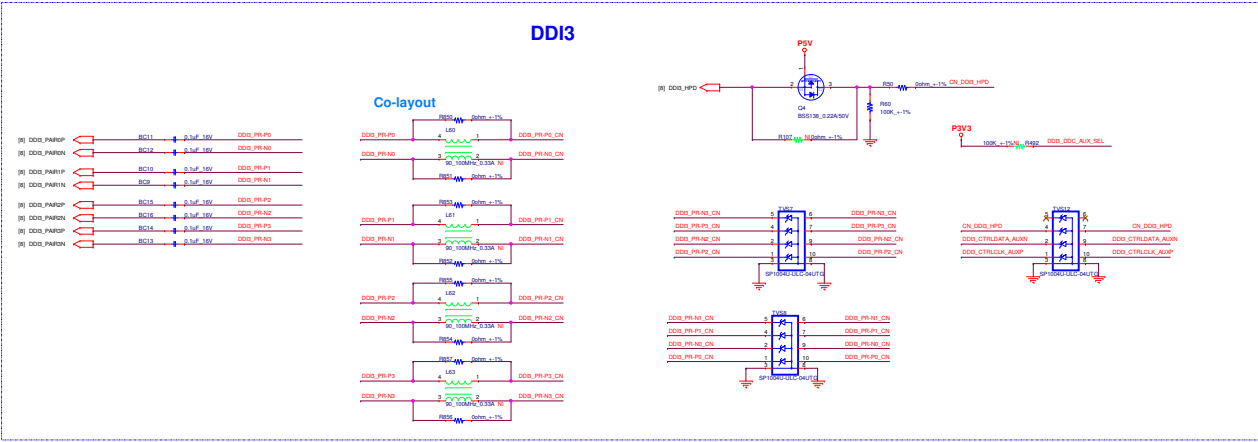


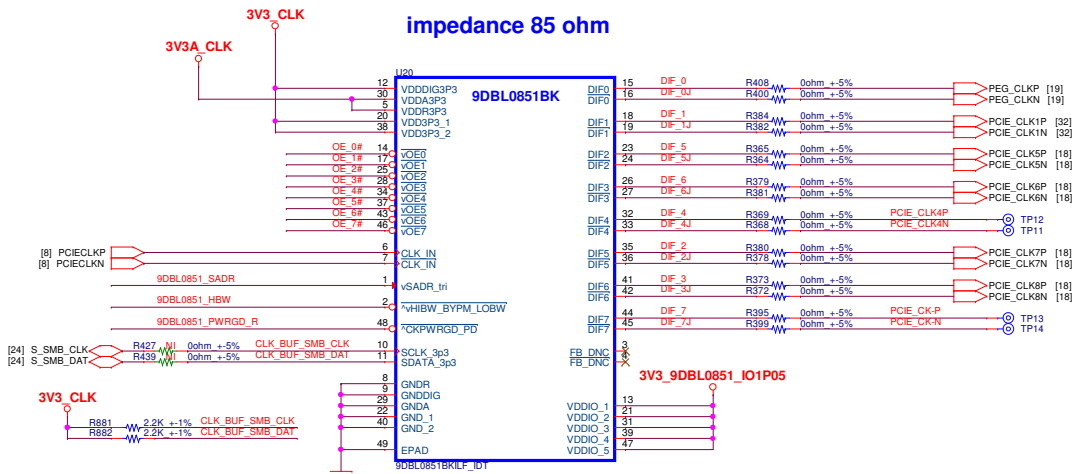
Table 4-1: Power Supply Rail Requirements

| Power Rail | 16 W Slot | 25 W Slot | 15W-ATX Power Connector | 75 W Slot |
|--------------------|---------------|---------------|-------------------------|---------------|
| +3.3V | | | | |
| Voltage tolerance | ± 9% (max) | ± 9% (max) | N/A | ± 9% (max) |
| Supply Current | 3.0 A (max) | 3.0 A (max) | N/A | 3.0 A (max) |
| Capacitive Load | 1000 uF (max) | 1000 uF (max) | N/A | 1000 uF (max) |
| +12V | | | | |
| Voltage tolerance | ± 8% | ± 8% | +5% / -8% (max) | ± 8% |
| Supply Current | 0.5 A (max) | 21 A (max) | 6.25 A (max) | 5.2 A (max) |
| Capacitive Load | 300 uF (max) | 1000 uF (max) | 2000 uF (max) | 2000 uF (max) |
| +3.3Vaux | | | | |
| Voltage tolerance | ± 9% (max) | ± 9% (max) | N/A | ± 9% (max) |
| Supply Current | 375 mA (max) | 375 mA (max) | N/A | 375 mA (max) |
| Wake-up Enabled | 20 mA (max) | 20 mA (max) | N/A | 20 mA (max) |
| Non-wakeup Enabled | 150 uF (max) | 150 uF (max) | N/A | 150 uF (max) |
| Capacitive Load | 150 uF (max) | 150 uF (max) | N/A | 150 uF (max) |

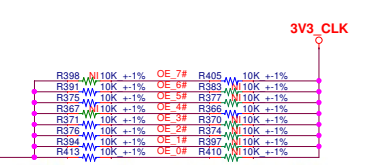
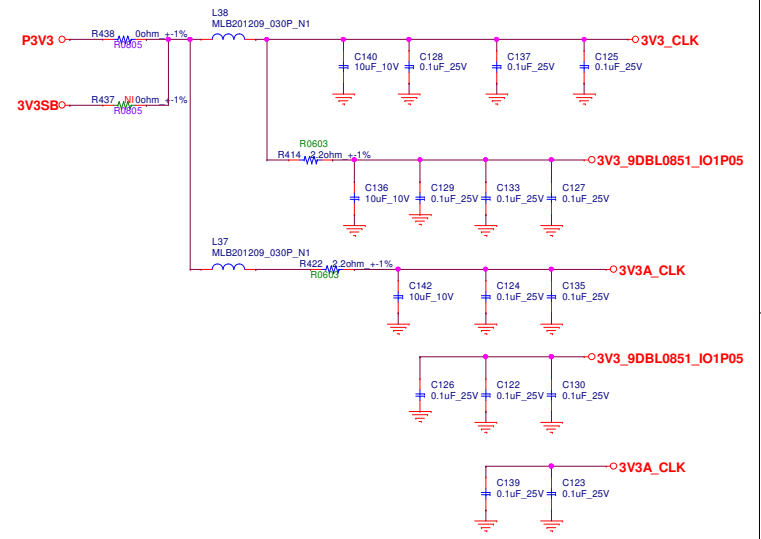
Notes:

- The maximum current draw rate for each add-in card shall be no more than 0.1 A/us.
- Each add-in card shall limit its bulk capacitance on each power rail to less than the values shown in Table 4-1.
- System boards that support Plug-and-play shall limit the voltage draw rate to that of the maximum current to the card shall not exceed the specified maximum current. This is calculated by the equation $\frac{dI}{dt} \leq \frac{I}{RC}$.
- The maximum voltage variation between +20V equals ± 1.00 V.





x16
x4
x1
x1
x1
x1



SMBus Address Selection Table

| State of SADR on first application of CKPWRGD_PD# | SADR | Address | + Read/Write bit |
|---|------|---------|------------------|
| 0 | 0 | 1101011 | X |
| M | M | 1101100 | X |
| 1 | 1 | 1101101 | X |

Note: If not using CKPWRGD (CKPWRGD tied to VDD3.3), all 3.3V VDD need to transition from 2.1V to 3.135V in <300usec.

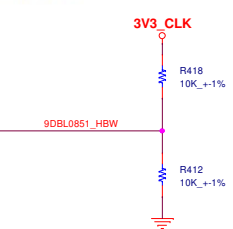
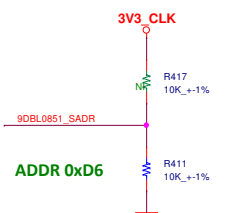
PLL Operating Mode

| HIBW BypM LoBW# | MODE | Byte1 [7:6] Readback | Byte1 [4:3] Control |
|-----------------|-----------|----------------------|---------------------|
| 0 | PLL Lo BW | 00 | 00 |
| M | Bypass | 01 | 01 |
| 1 | PLL Hi BW | 11 | 11 |

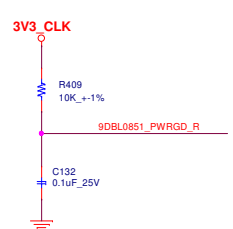
Power Management Table

| CKPWRGD_PD# | CLK_IN | SMBus OEx bit | OEx# Pin | DIFx | | PLL |
|-------------|---------|---------------|----------|------------------|------------------|-----------------|
| | | | | True O/P | Comp. O/P | |
| 0 | X | X | X | Low ¹ | Low ¹ | Off |
| 1 | Running | 0 | X | Low ¹ | Low ¹ | On ² |
| 1 | Running | 1 | 0 | Running | Running | On ² |
| 1 | Running | 1 | 1 | Low ¹ | Low ¹ | On ² |

- The output state is set by B11[1:0] (Low/Low default)
- If Bypass mode is selected, the PLL will be off, and outputs will be running.



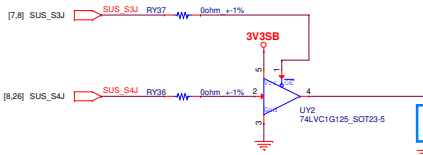
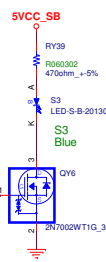
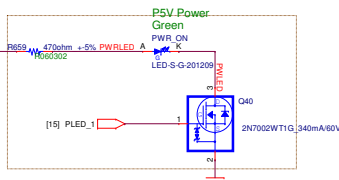
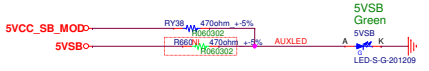
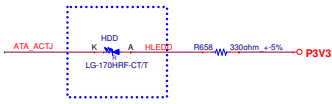
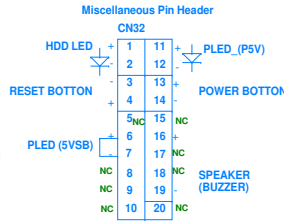
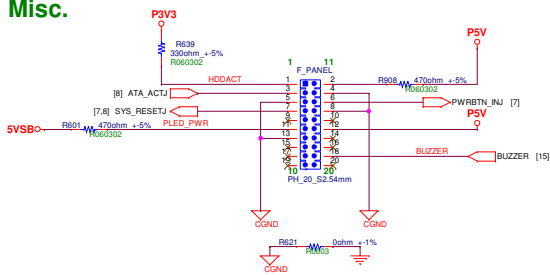
Remove LPC CLK BUFFER



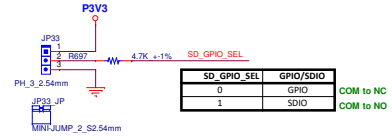
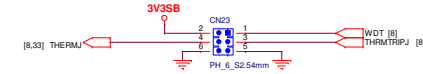
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| | | | |
|--------|-----------------------------|--------------|----------|
| Title | | Clock Buffer | |
| Size | Document Number | Rev | A1 |
| Custom | Express-BASE6 R3.1 | | |
| Date: | Saturday, December 03, 2022 | Sheet | 20 of 38 |

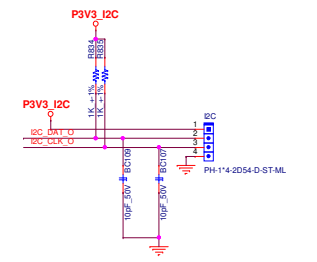
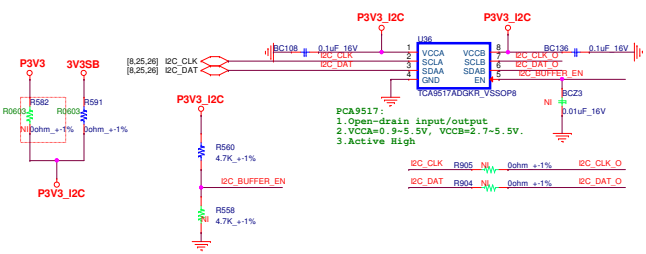
Misc.



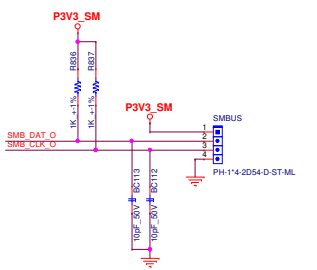
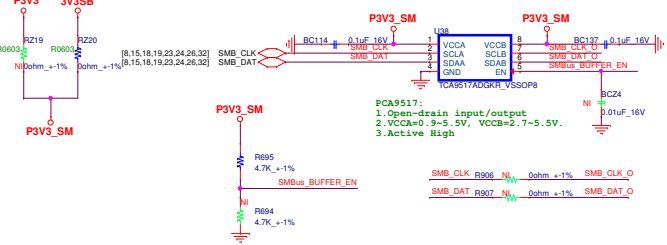
| OE# | A | Output |
|-----------|---|--------|
| [SUS_S3J] | H | H |
| [SUS_S4J] | L | L |
| [SUS_S4J] | H | X |
| [SUS_S4J] | L | Z |



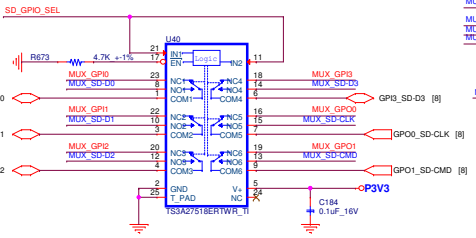
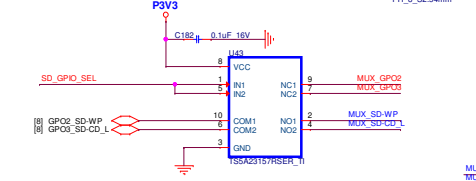
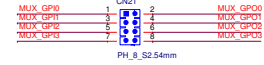
I2C I2C BUFFER



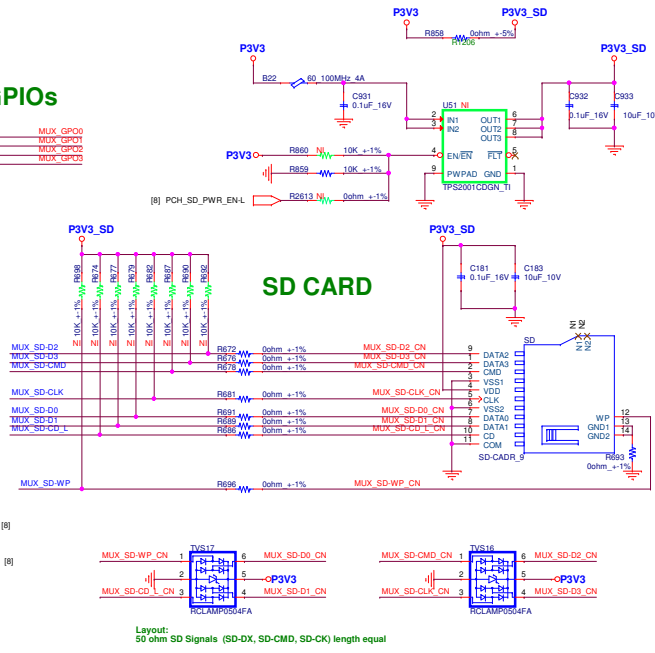
SMBus SMBus BUFFER



Module GPIOs

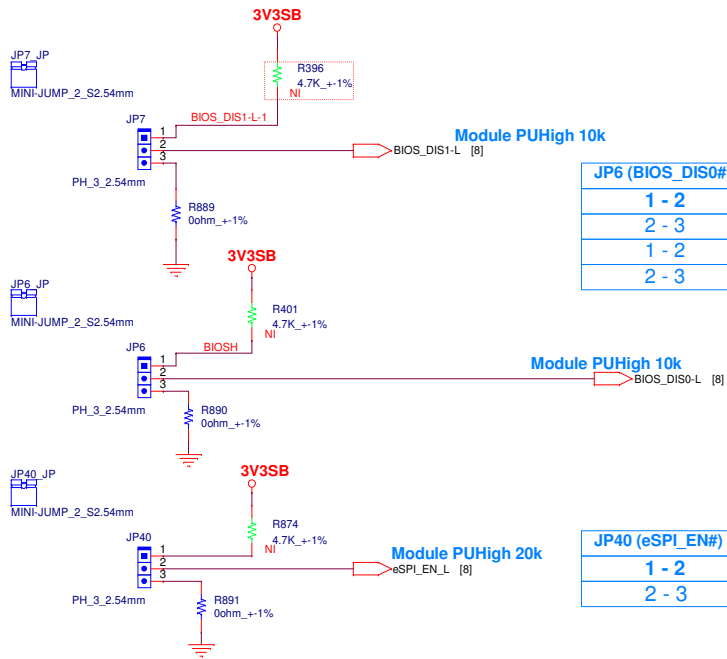


SD CARD



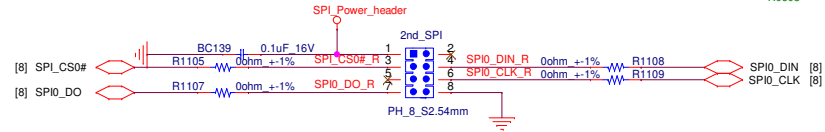
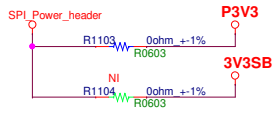
Layout: 50 ohm SD Signals (SD-DX, SD-CMD, SD-CK) length equal

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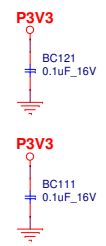
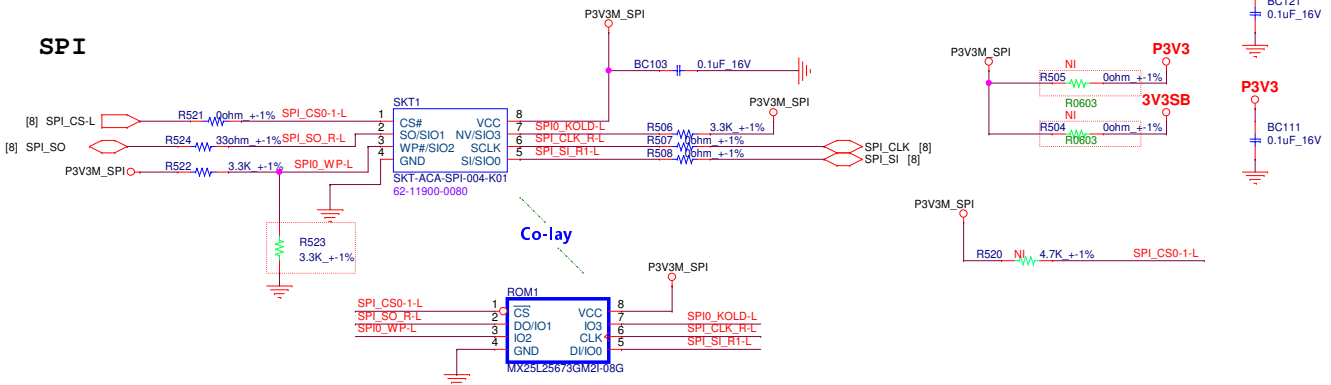


| JP6 (eSPI_EN#) | JP7 (BIOS_DIS1#) | BIOS Boot Device Select |
|----------------|------------------|--------------------------------------|
| 1 - 2 | 1 - 2 | Module SPI0 / SPI1 |
| 2 - 3 | 1 - 2 | FWH on Carrier (on longer supported) |
| 1 - 2 | 2 - 3 | Module SPI0 / Carrier SPI1 |
| 2 - 3 | 2 - 3 | Carrier SPI0 / Module SPI1 |

| JP40 (eSPI_EN#) | BIOS Boot Device Select |
|-----------------|---------------------------|
| 1 - 2 | LPC Mode (default) |
| 2 - 3 | eSPI mode |



SPI

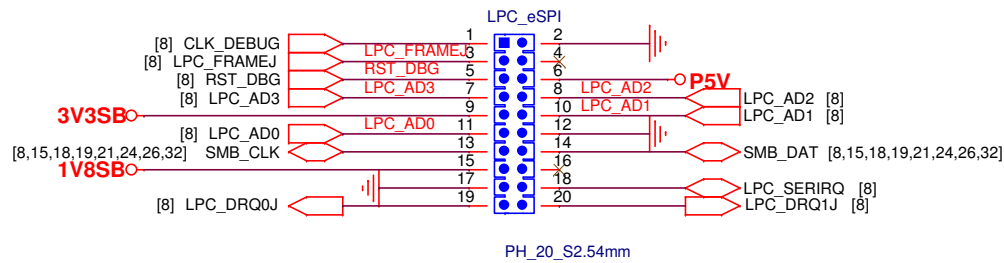



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|--|--|------------------|
| Title External BIOS& SPI connector | | |
| Size A3 | Document Number Express-BASE6 R3.1 | Rev A1 |
| Date: Saturday, December 03, 2022 Sheet 22 of 38 | | |

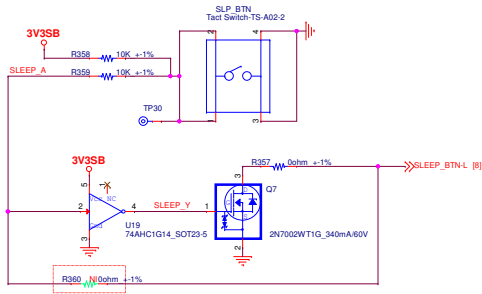
Reference Spec.
 Installable LPC Debug Module Design Guide

Debug Header (LPC / ESPI)



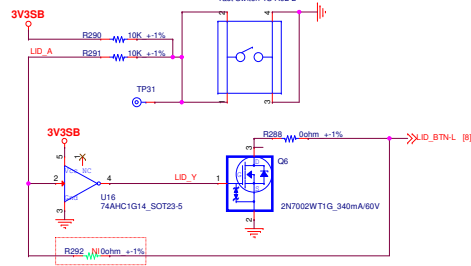
| | | | |
|---|---|---|------------------|
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| | | Title LPC Debug Module | |
| Size A4 | Document Number Express-BASE6 R3.1 | | Rev A1 |
| Date: Saturday, December 03, 2022 Sheet 23 of 38 | | | |

SLEEP BTN

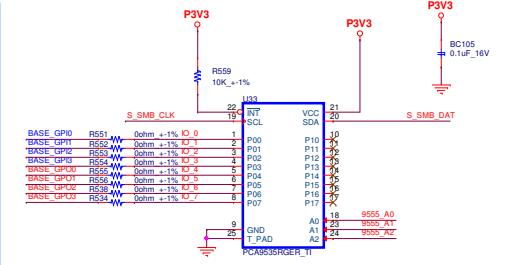
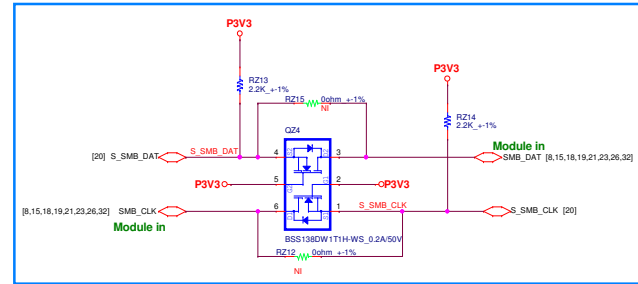
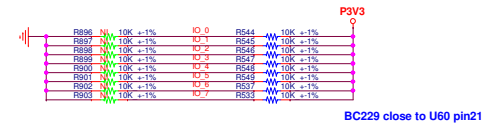
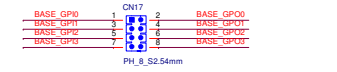


LID BTN

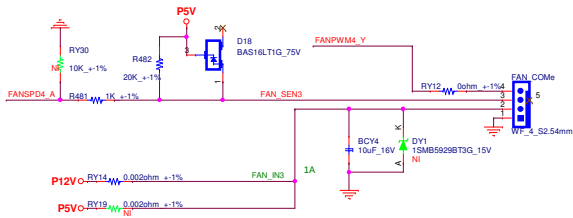
Type 6 Add



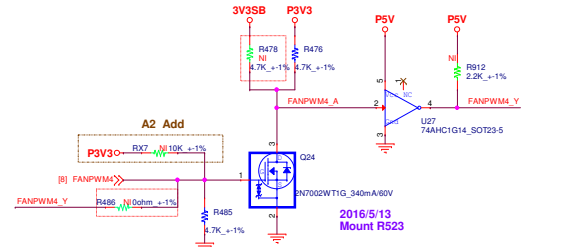
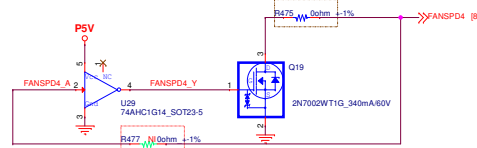
SMBUS_GPIO (base)



FAN(from module)

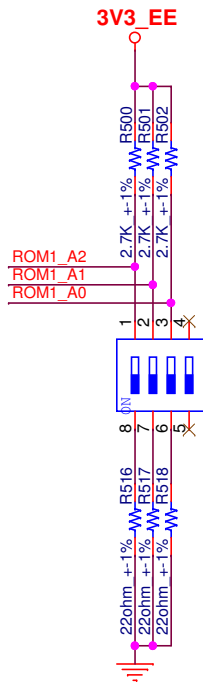


A2 BOM Change



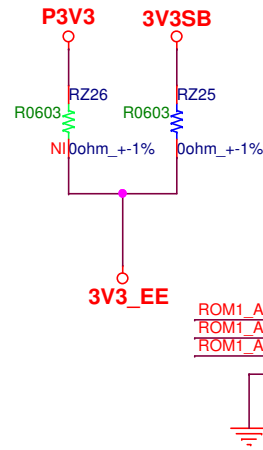
GPIO Address : 40h

I2C EEPROM



| SW I2C EEPROM U32 | |
|-------------------|---------------|
| 1-8 | A2_ON (LOW) |
| 2-7 | A1_OFF (High) |
| 3-6 | A0_ON (LOW) |

Address: A4h



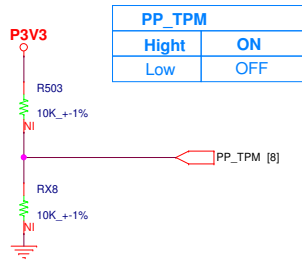
| Package | Device Type Identifier | | | | Hardware Client Address Bits | | | R/W Select |
|--------------------------|------------------------|-------|-------|-------|------------------------------|-------|-------|-------------|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| SOIC, TSSOP, UDFN, VFBGA | 1 | 0 | 1 | 0 | A2 | A1 | A0 | R \bar{W} |

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| | | |
|----------------|--------------------|-----|
| Title | | |
| I2C Eeprom,LPC | | |
| Size | Document Number | Rev |
| A4 | Express-BASE6 R3.1 | A1 |

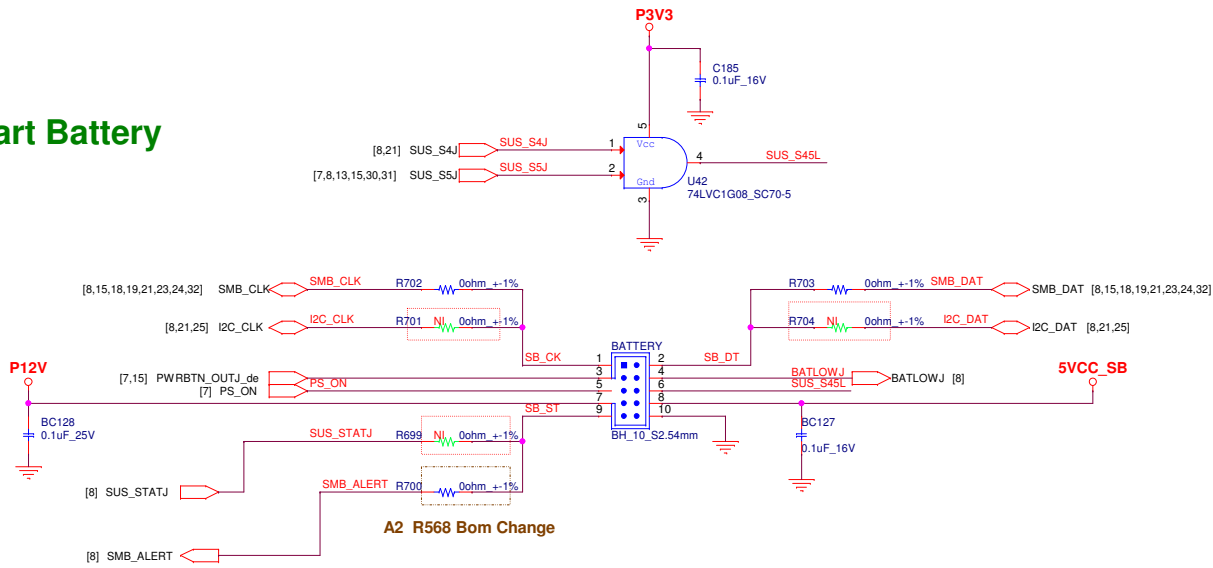
Date: Saturday, December 03, 2022 Sheet 25 of 38

PP_TPM



| PP_TPM | |
|--------|-----|
| High | ON |
| Low | OFF |

Smart Battery



| | | | |
|-----------------------------------|--|--|--|
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| | | Title: TPM&Smart Battery | |
| Size: A3 | Document Number: Express-BASE6 R3.1 | Rev: A1 | |
| Date: Saturday, December 03, 2022 | Sheet: 26 | of 38 | |

Layout Note:
Route all 0R0 jumpers as Tripads
Keep stubs as short as possible

Note: LVDS A usage (default)
LVDS A = 0R0
eDP0 = NI

Note: eDP0 usage (option)
LVDS A = NI
eDP0 = 0R0

Note:
There will be at least two different BOMs
One will support LVDS interface
The other will support eDP

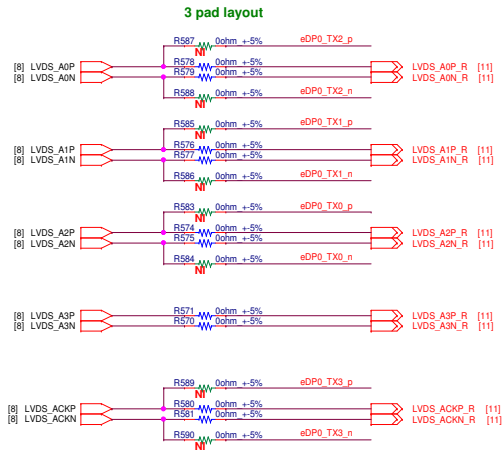
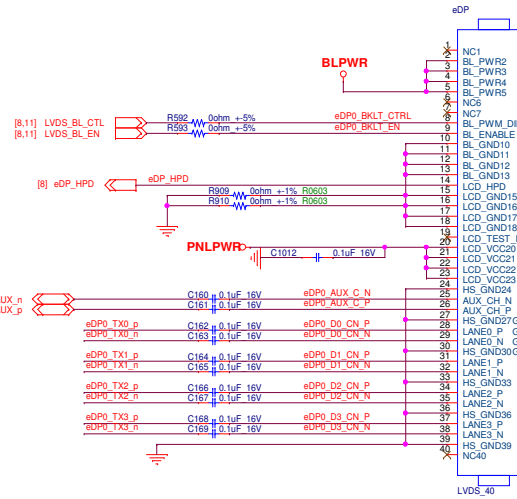
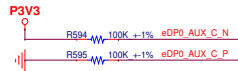
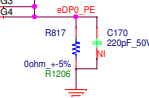


Table 4.36: LVDS / eDP Pin Assignment

| Pin Name | Type 6/10 Pin Number | eDP |
|----------------|----------------------|---------------|
| LVDS_A0+ | A71 | eDP_TX2+ |
| LVDS_A0- | A72 | eDP_TX2- |
| LVDS_A1+ | A73 | eDP_TX1+ |
| LVDS_A1- | A74 | eDP_TX1- |
| LVDS_A2+ | A75 | eDP_TX0+ |
| LVDS_A2- | A76 | eDP_TX0- |
| LVDS_A0K+ | A81 | eDP_TX3+ |
| LVDS_A0K- | A82 | eDP_TX3- |
| LVDS_VDD_EN | A77 | eDP_VDD_EN |
| LVDS_BKLT_EN | B79 | eDP_BKLT_EN |
| LVDS_DIC_OK | A83 | eDP_AUX+ |
| LVDS_DIC_DAT | A84 | eDP_AUX- |
| LVDS_BKLT_CTRL | B83 | eDP_BKLT_CTRL |
| RSVD | A87 | eDP_HPD |



40-Pin eDP connector



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| | | | |
|--------|-----------------------------|--------------------|----------|
| File | | eDP | |
| Size | Document Number | Express-BASE6 R3.1 | |
| Custom | | Rev | A1 |
| Date: | Saturday, December 03, 2022 | Sheet | 27 of 38 |

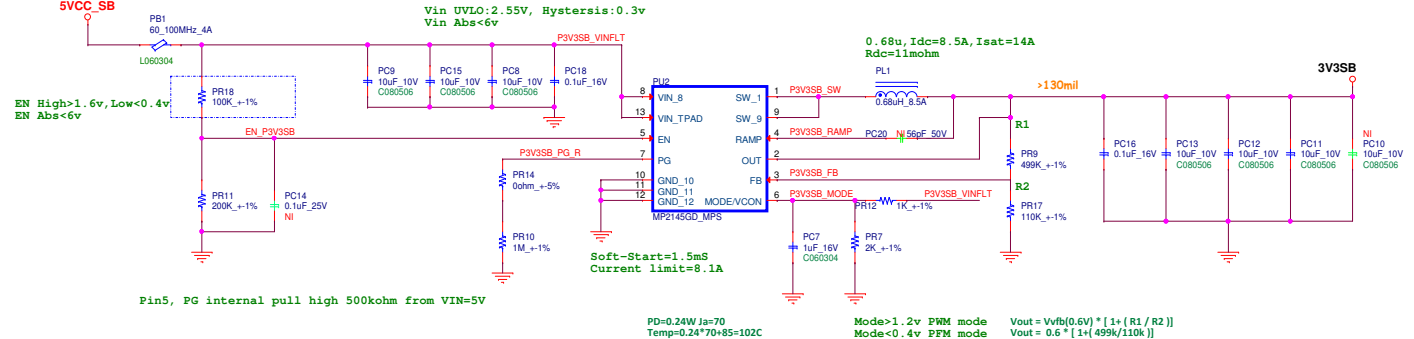
P5VSB to 3V3SB

P3V3SB(MP2145)

P3V3SB Specification:
 Vout: 3.30V
 I_{max}: 2A
 I_{step}: 1A
 Slew Rate: 2.5A/uS
 TOB: + - 5.0%
 Switching Frequency per Phase: 1.2MHZ

MP2145 power sequence
 1. VIN
 2. EN
 3. Output

5V/1.65A@eff80%



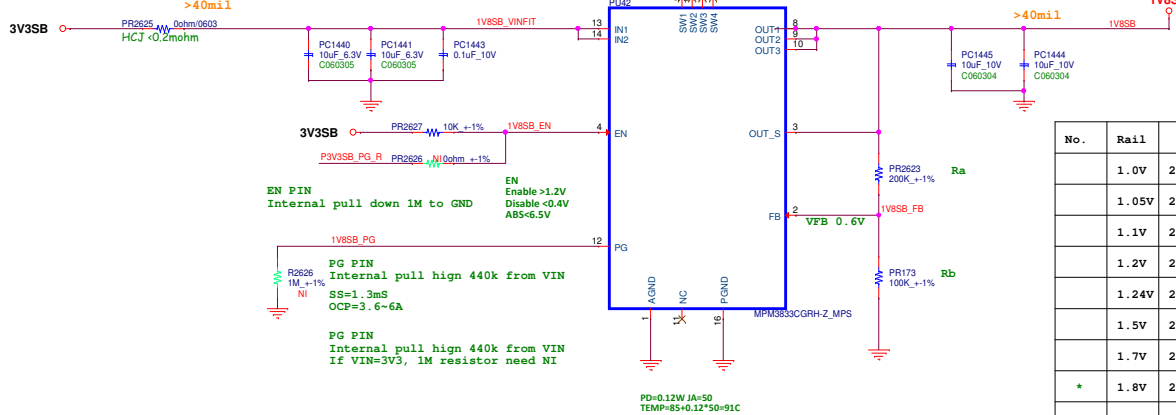
1V8SB (MPM3833C)

1V8SB Specification:
 Vout: 1.8V
 I_{max}: 0.6A
 I_{step}: 0.3A
 Slew Rate: 2.5A/uS
 TOB: + - 5.0%
 Switching Frequency per Phase: 1.15MHZ

MPM3833C power sequence
 1. VIN
 2. PIN9 EN
 3. Output
 4. PIN8 PG

3.3V

0.363A@VIN=3.3V, 90%eff



| No. | Rail | Ra | Rb | Vout |
|-----|-------|------|-------|---------|
| | 1.0V | 200k | 300k | 1.000V |
| | 1.05V | 200k | 267k | 1.049V |
| | 1.1V | 200k | 240k | 1.100V |
| | 1.2V | 200k | 200k | 1.200V |
| | 1.24V | 200k | 187k | 1.2417V |
| | 1.5V | 200k | 133k | 1.502V |
| | 1.7V | 200k | 107k | 1.721V |
| * | 1.8V | 200k | 100k | 1.800V |
| | 2.5V | 200k | 61.9k | 2.5386V |
| | 3.3V | 200k | 44.2k | 3.3149V |


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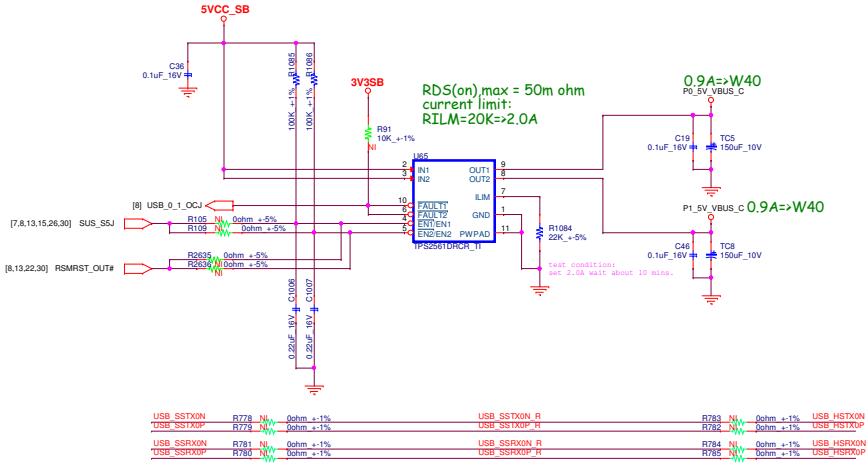
Title: Power(5VSB to 3VSB) & 1V8SB
 Size C Document Number: Express-BASE6 R3.1 Rev A1
 Date: Saturday, December 03, 2022 Sheet 26 of 38

A3 Change -
2012/02/29
Change new power solution of P12V to P3V3
1. Remove U3(76-03728-50Z0)
2. Add UY120(76-00417-50Z0)(SC417)

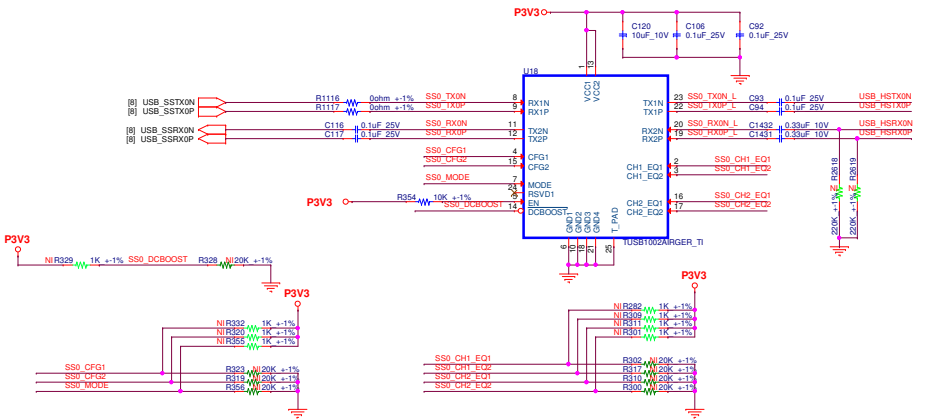
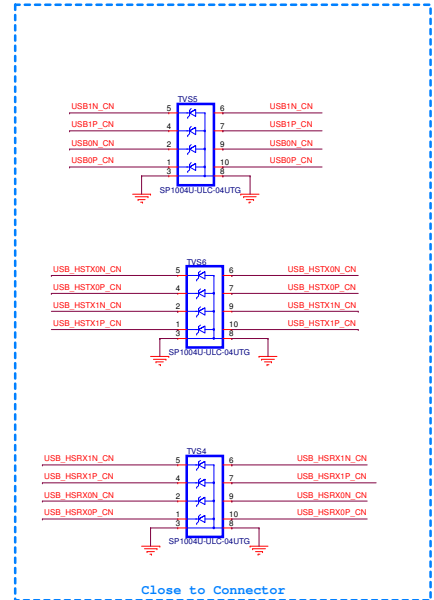
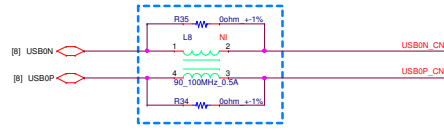
B1 Change -
2012/12/26
Power Solutions to fine turn
1. RY50 change from 10 ohm (64-10R05-4490)(0402) to 0 ohm(63-R0003-4510)(0603)
2013/01/03
1. BCY1017 Remove 100pF(78-10134-14A0)(0402)

C1 Change -
20200907
1. Remove DC to DC P3V3 solution, and PSU direct to provide P3V3 (All)

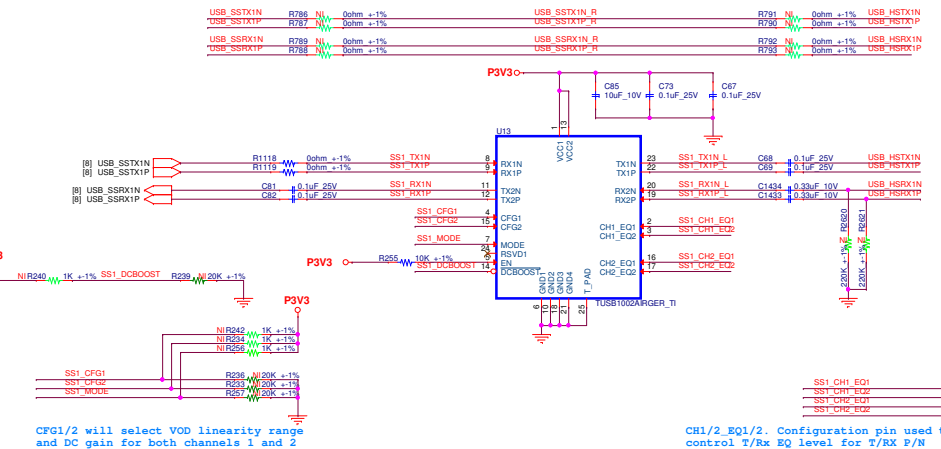
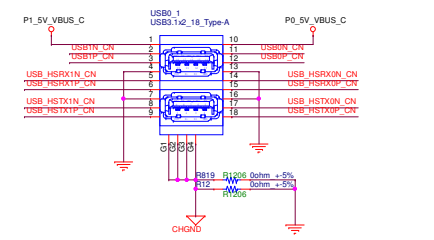
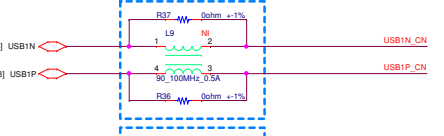
| | | |
|---|--|---|
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| Title Reserved | | |
| Size B | Document Number Express-BASE6 R3.1 | Rev A1 |
| Date: Saturday, December 03, 2022 | Sheet 1 | of 29 |

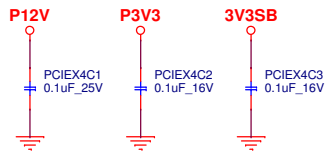


PCB CO-LAYOUT



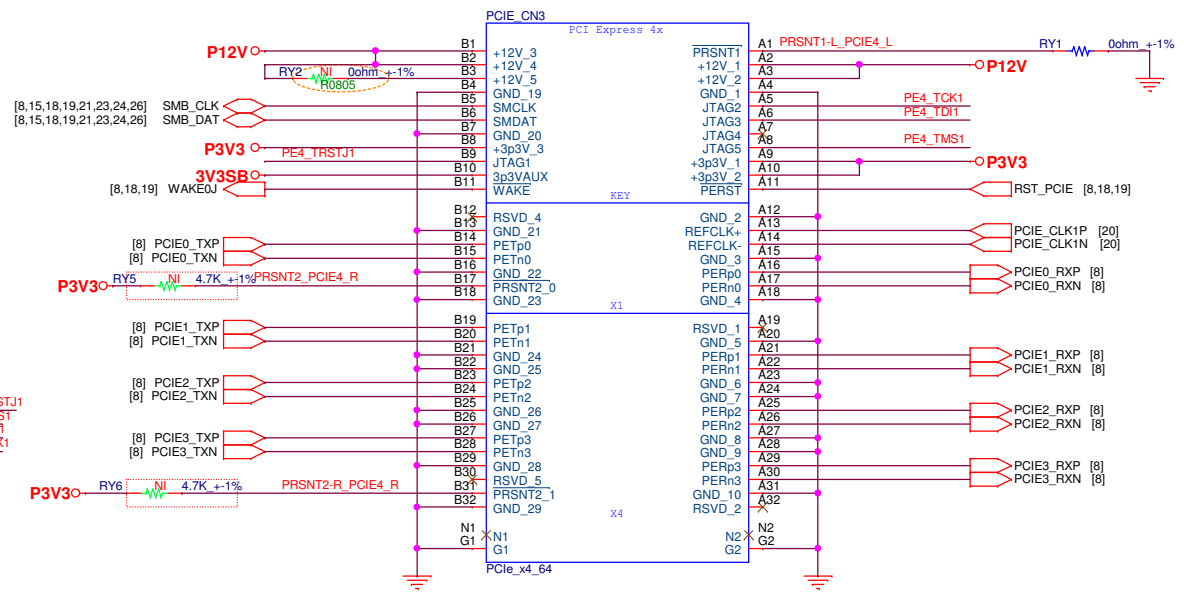
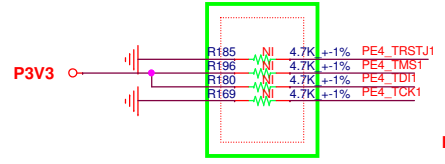
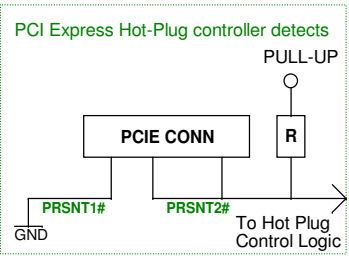
PCB CO-LAYOUT





EMI request 20160421

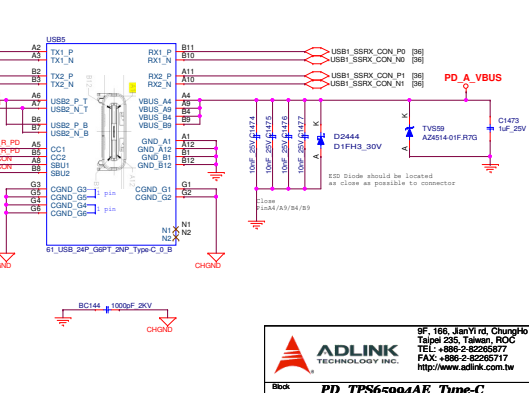
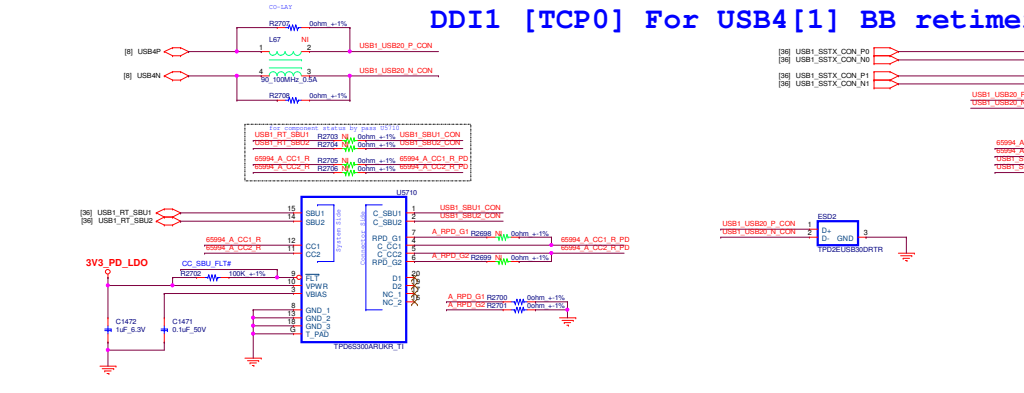
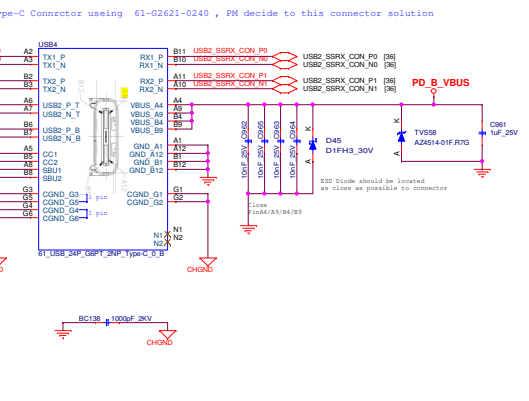
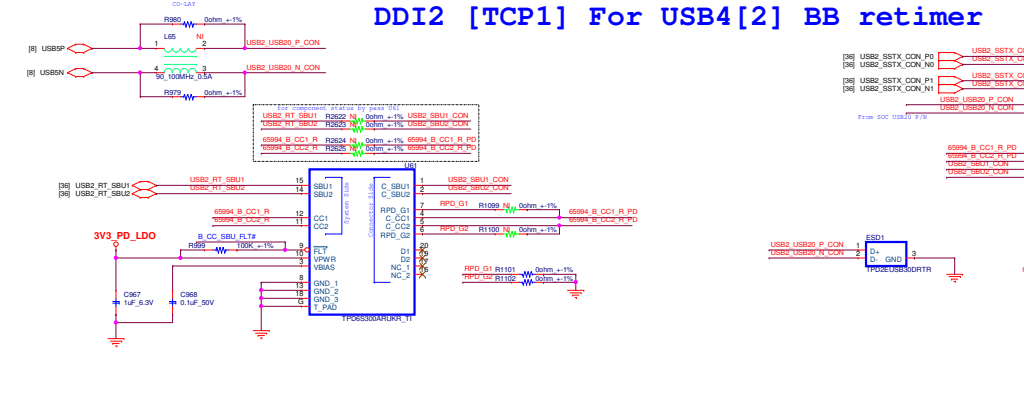
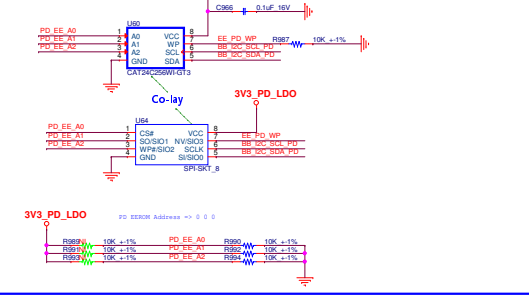
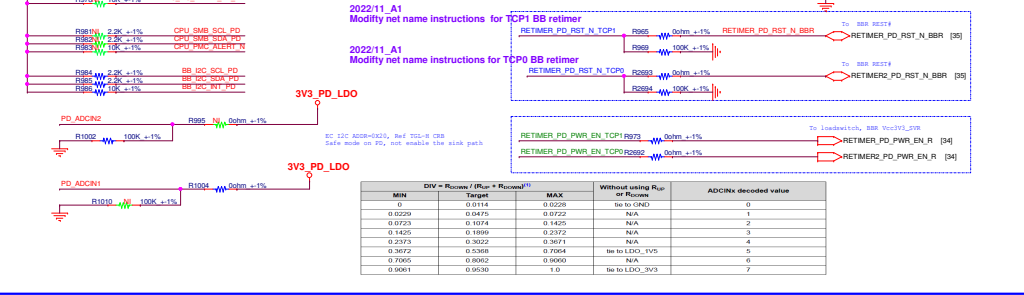
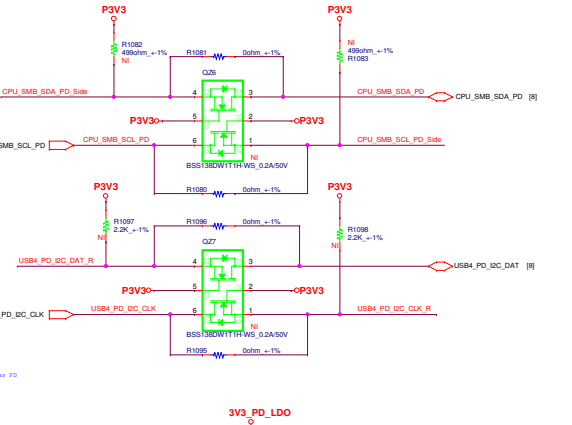
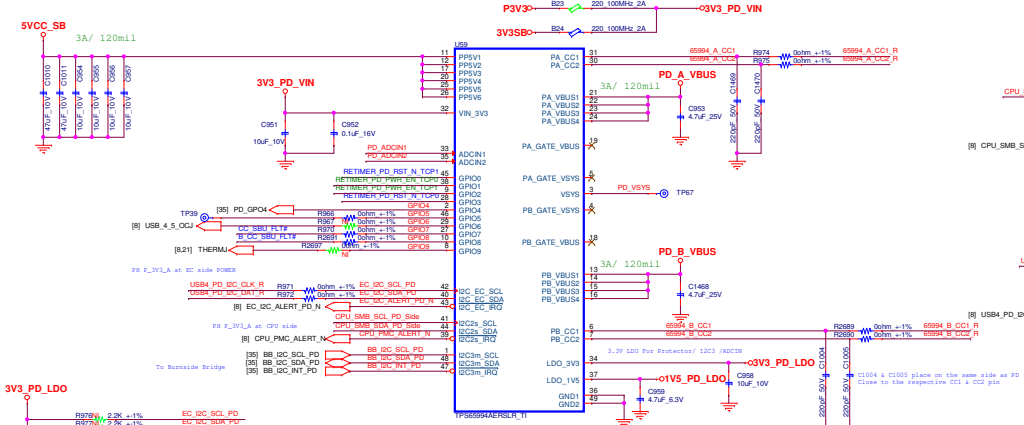
PCIe X4 SMT GEN4 SLOT : 61-L1000-0640



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| | | |
|------------------------|-----------------------------|----------------|
| Title | | |
| PCI EXPRESS x 4 | | |
| Size | Document Number | Rev |
| Custom | Express-BASE6 R3.1 | A1 |
| Date: | Saturday, December 03, 2022 | Sheet 32 of 38 |



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Block **PD_TPS65994AE_Type-C**

Size **41x21mm** Project Name **Express-BASE6 R3.1** Rev A1

Date: Saturday, December 6, 2020 15:33:58

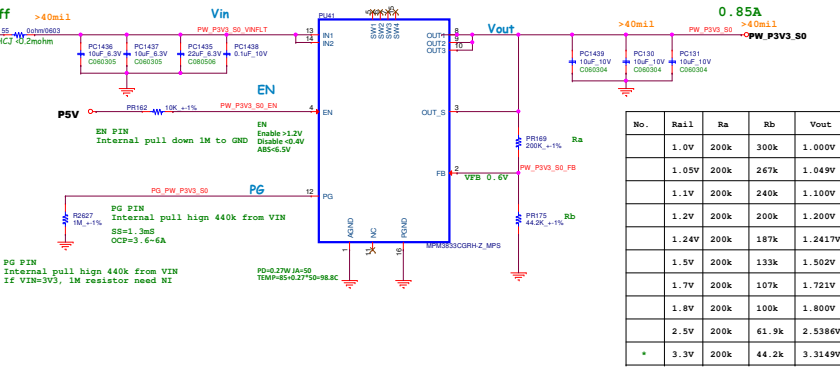
PW_P3V3_S0 (MPM3833C)

PW_P3V3_S0 Specification:
 Vout: 3.30V
 Imax: 0.85A
 Istep: 0.42A
 Slew Rate: 2.5A/uS
 TOB: + - 5.0%
 Switching Frequency per Phase: 1.15MHz

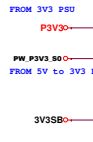
MPM3833C power sequence
 1. VIN
 2. PIN9 EN
 3. Output
 4. PIN8 PG

5V FROM PSU 5V

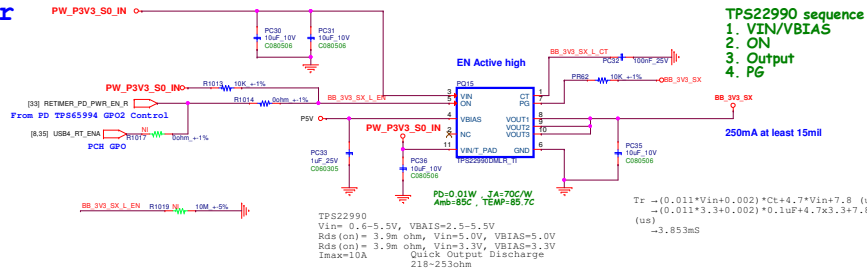
0.616A@VIN=5V,91%eff



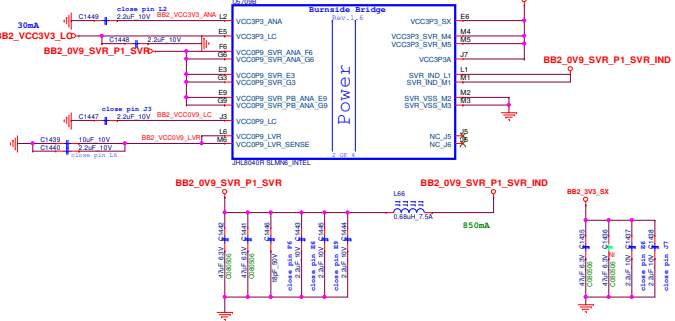
DDI2 [TCP1] For USB4 BB retimer



Note
 To support vPRO Docking PW_P3V3_SX Should be always on even at S5.
 To support vPRO Docking PD FW Should support vPRO Alternate mode and use vPRO.

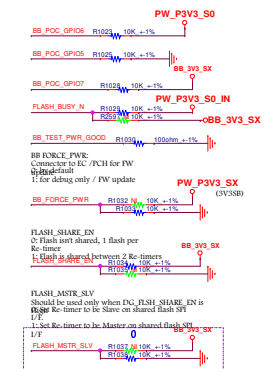
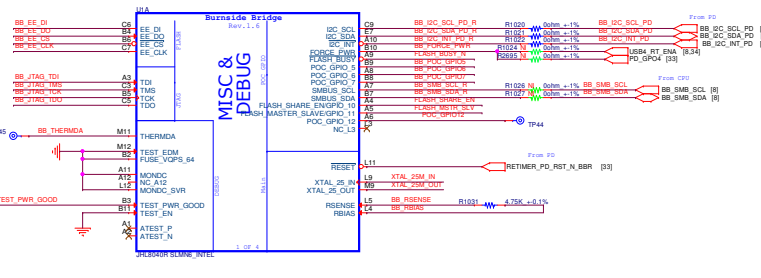


DDI1 [TCP0] For USB4 BB retimer

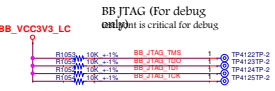
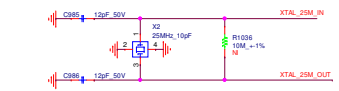


DDI2 [TCP1] For USB4 BB retimer

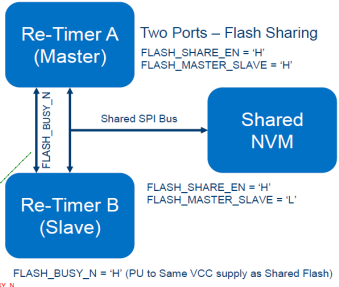
HW Pull Up/ Pull Down of BBR



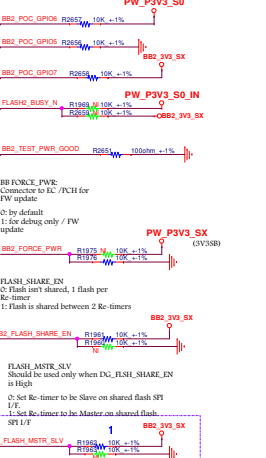
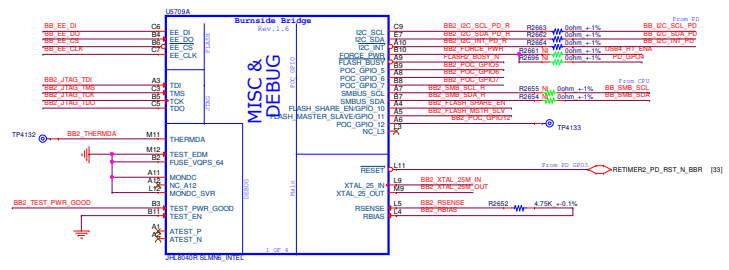
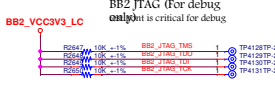
2022/11_A1
1. remove R1037, upload R1038 beTCP1 (DDI2) slave retimer



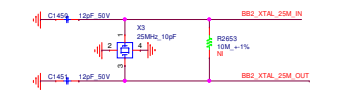
Re-Timer - Flash Sharing



DDI1 [TCP0] For USB4 BB retimer



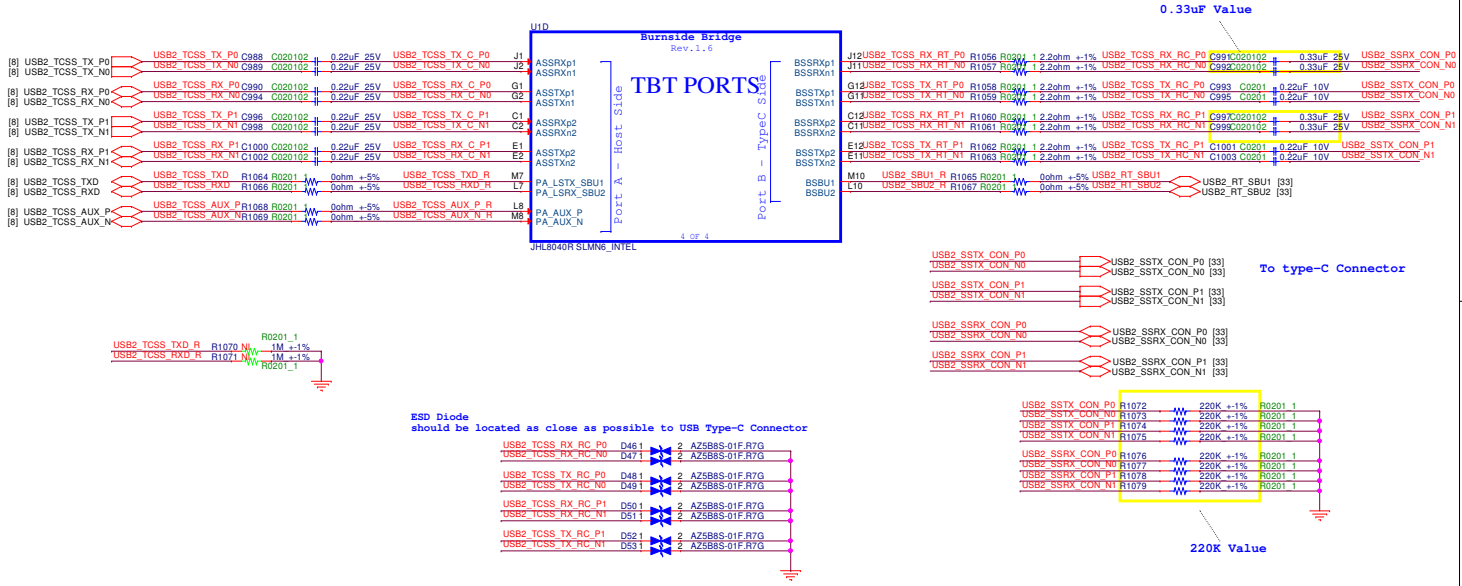
2022/11_A1
1. remove R1963, upload R1962 beTCP0 (DDI1) Master retimer



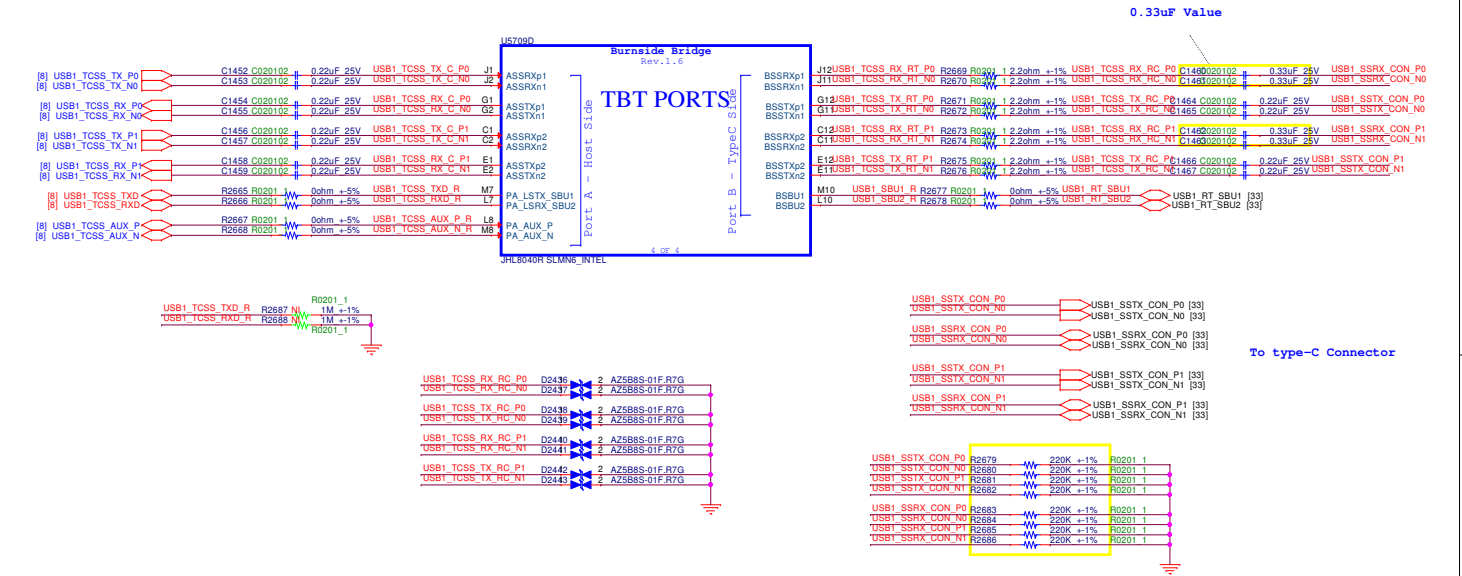
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DDI2 For USB4 BB retimer

Package 0201 Placement and value need to adjust!



DDI1 For USB4 BB retimer



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Block: **Burnside Bridge_TBT Port**

| | | |
|----------|-----------------------------|----------------|
| Size | Project Name | Rev |
| Customer | Express-BASE6 R3.1 | A1 |
| Date: | Saturday, December 03, 2022 | Sheet 36 of 38 |

Vendor : ADLINK
Part Name : Type 6 carrier board

Schematic Version : A1


| Revision | Date | Author | Change Content | Reason for modify | Note |
|----------|------|--------|----------------|-------------------|------|
| | | | | | |
| | | | | | |
| | | | | | |

| | | |
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| Block Change_History | | |
| Size | Project Name | Rev |
| A3 | Express-BASE6 R3.1 | A1 |
| Date: | Saturday, December 03, 2022 | Sheet 37 of 38 |

Vendor : ADLINK
Part Name : Type 6 carrier board

Schematic Version : A1

| Page | Date | Change Description | Note |
|---------|------------|---|------|
| Page.7 | 2022/10/31 | A2 PCB modify add 5VB jumper pin header for module power, and discuss A2 spec and lock down. | |
| Page.15 | 2022/10/31 | A2 PCB modify it . (Modify SIO strap pin isolation design) | |
| Page.15 | 2022/10/31 | A2 PCB modify ; Change design to use disconnect CLK_SIO and achieve the function of enable or disable it. | |
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|---|---------------------------------|---|-----------|
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| Block | Next version change item | | |
| Size | Project Name | | Rev |
| Custom | Express-BASE6 R3.1 | | A1 |
| Date: | Saturday, December 03, 2022 | Sheet | 39 of 38 |