

Express-BASE7 Rev.A2

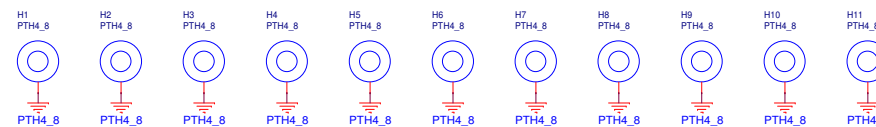
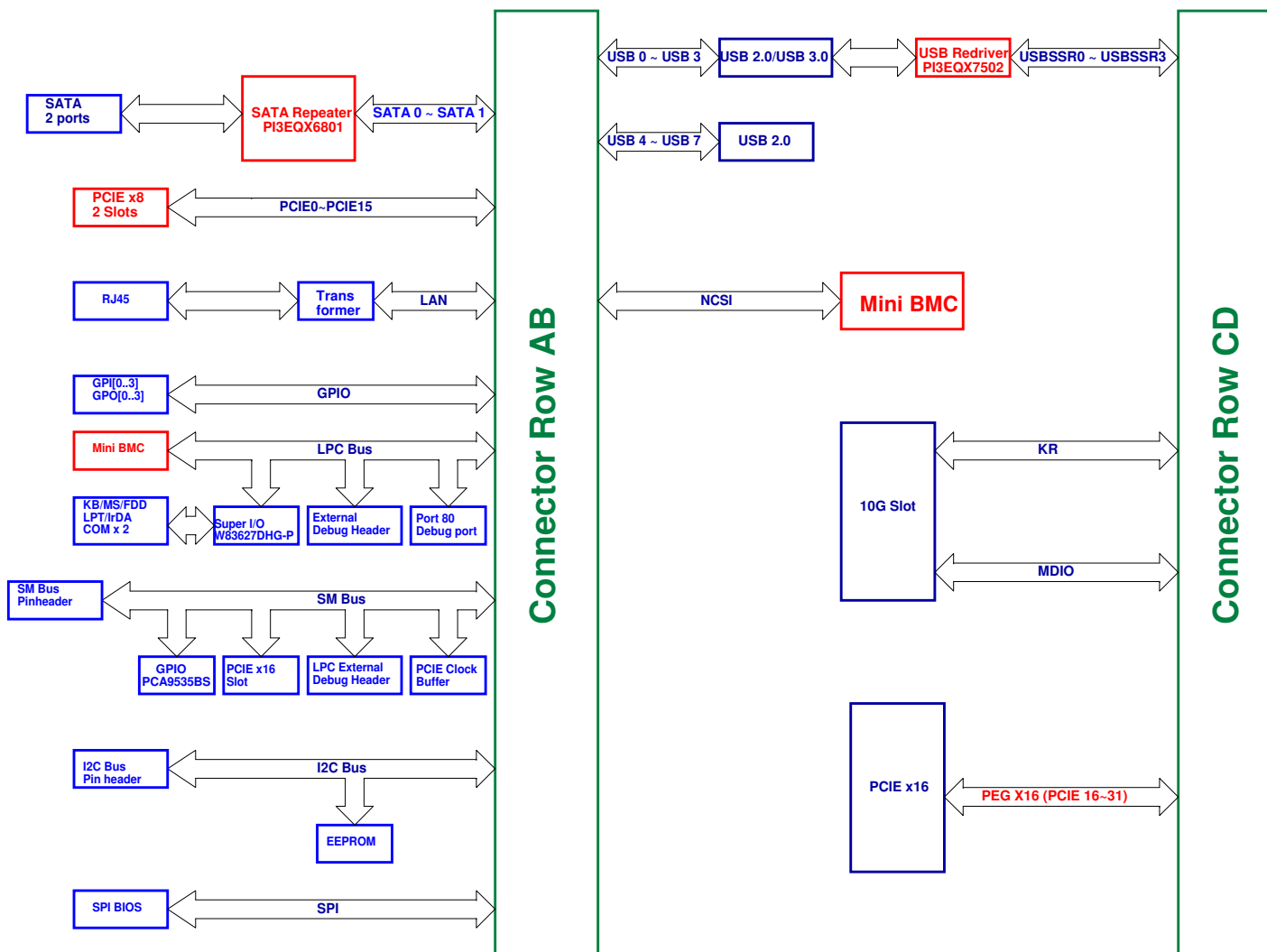
COM-Express Base Board
PICMG COM.0 Rev 2.0

PCB Size : 304.8 mm x 243.84 mm

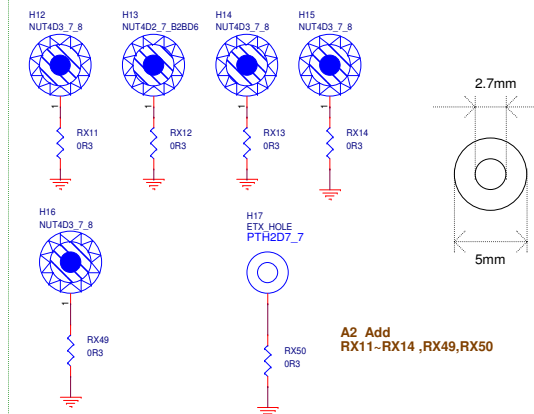
(12000mils x 9600mils)

ADLINK P/N : 51-77105-0A20

Block Diagram



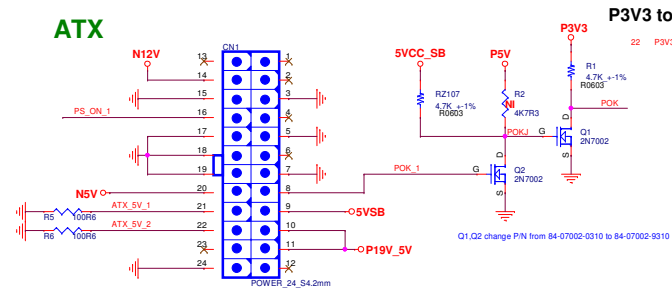
COM-Express Screw Hole



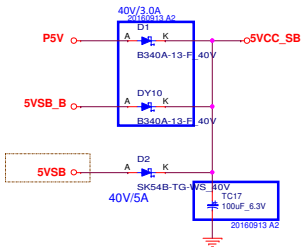
ADLINK TECHNOLOGY INC.
9F, 166, JianYi rd, ChungHo city, Taipei 235, Taiwan, ROC
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File
Cover Page
Size C
Document Number
Express-BASE7
Rev A2
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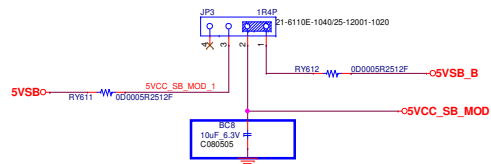
ATX



JP1 Power Type	
1-2	ATX Type
2-3	AT Type



JP3 5VSB to Module Source	
1-2	5VSB produced on Carrier from Vcc
2-3	5VSB from ATX Power Supply
3-4	No 5VSB to Module

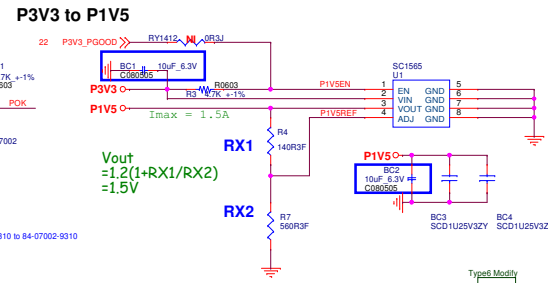


Power strategies	JP1	JP2	JP3	JP4
ATX PSU / ATX to Module	1-2	1-2	2-3	1-2
ATX PSU / AT to Module	2-3	1-2	3-4	2-3
AT PSU / ATX to Module	1-2	1-2	1-2	1-2
AT PSU / AT to Module	2-3	1-2	3-4	2-3

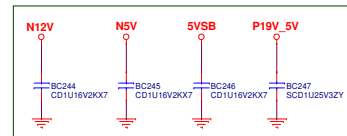
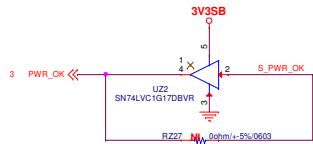
JP1 Power Type	
1-2	ATX Type
2-3	AT Type

JP2 Power button active	
1-2	SUS_S3#
2-3	SUS_S5#

P3V3 to P1V5



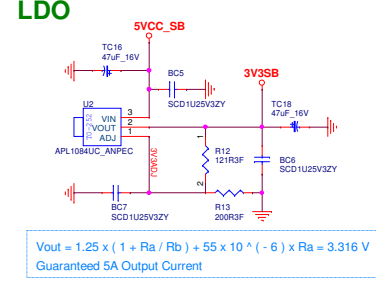
JP2 Power button active	
1-2	SUS_S3#
2-3	SUS_S5#



Type 7 Modify: EMI request 20160421

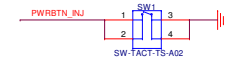
A2 Change -
2016/09/13
Change TC1,TC2,TC4,TC5,TC6,TC7,TC8,TC9,TC16,TC18 to 80-47611-6600
Change TC17 to 80-10710-7300
Change D1,DY10 to 83-3R004-09M0

LDO

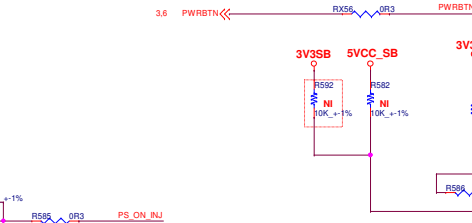
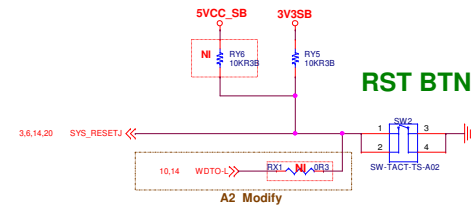


$V_{out} = 1.25 \times (1 + R_a / R_b) + 55 \times 10^{-6} \times R_a = 3.316 \text{ V}$
Guaranteed 5A Output Current

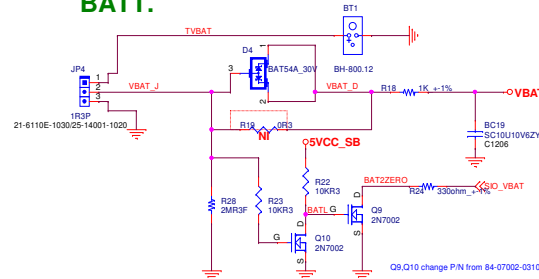
PWR BTN

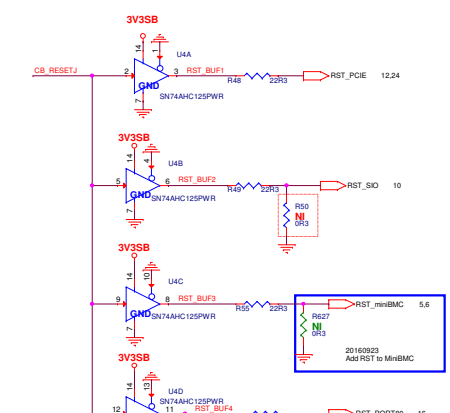
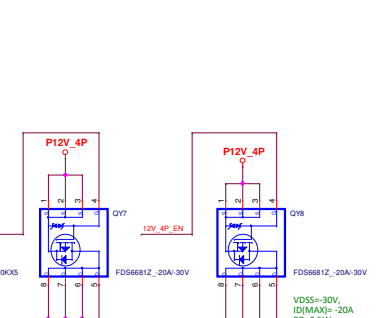
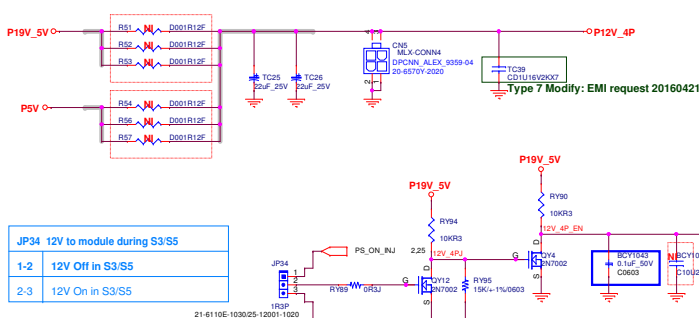
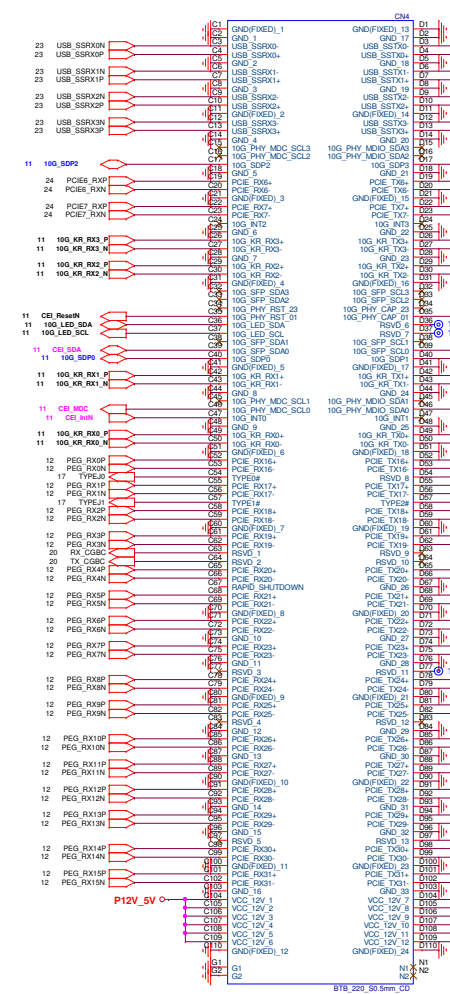
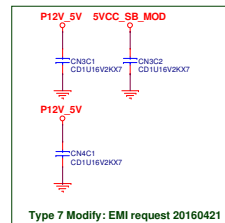
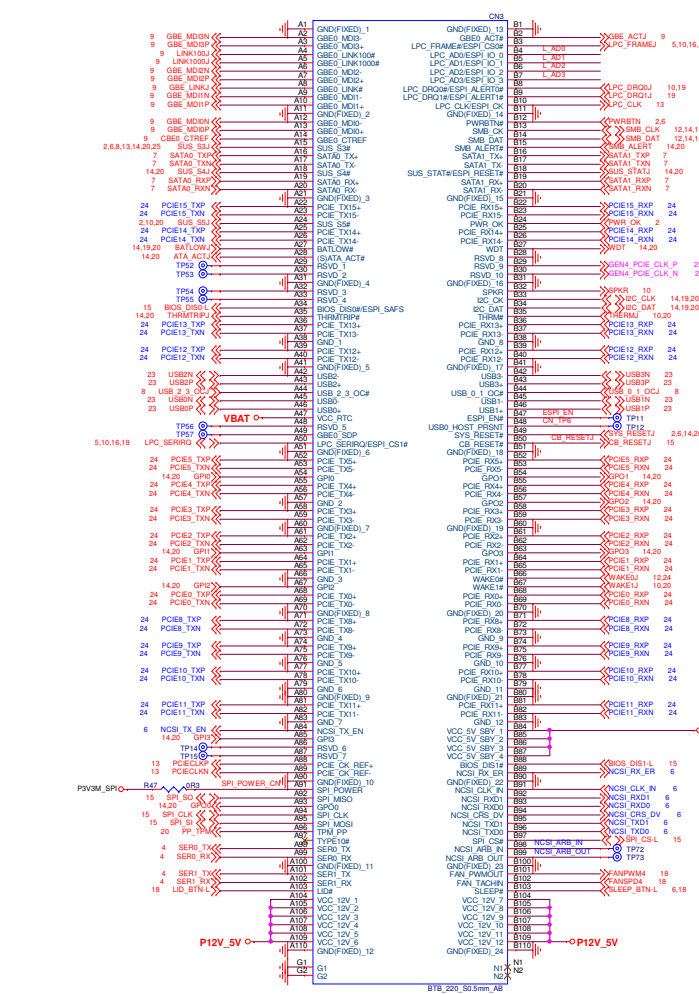


RST BTN



BATT.





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COM Express Connector

Express-BASE7

File: ...

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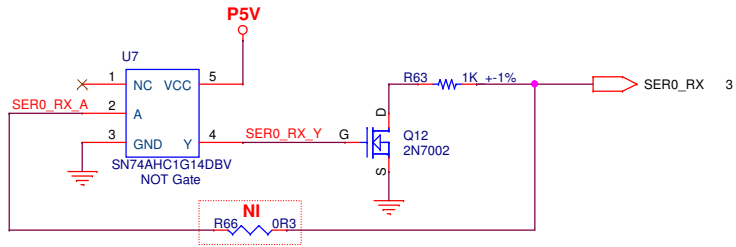
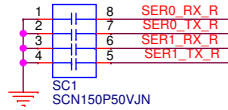
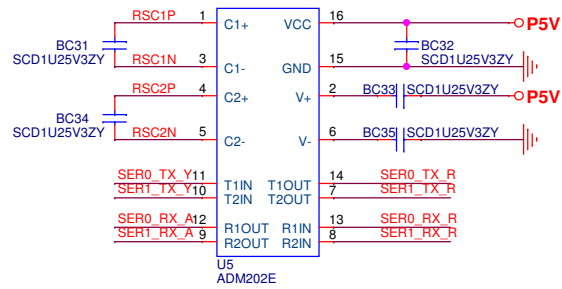
BP: 165, JimYi rd, Chungli city, Taipei 225, Taiwan, ROC

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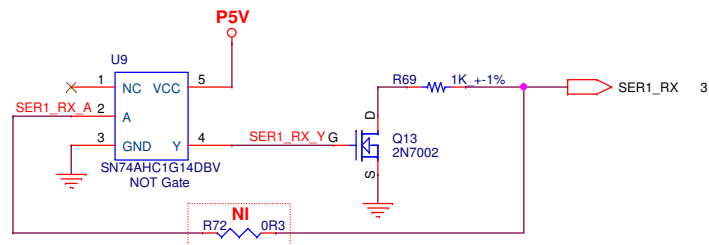
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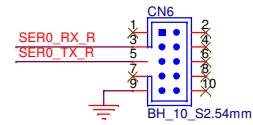
RS232 from module



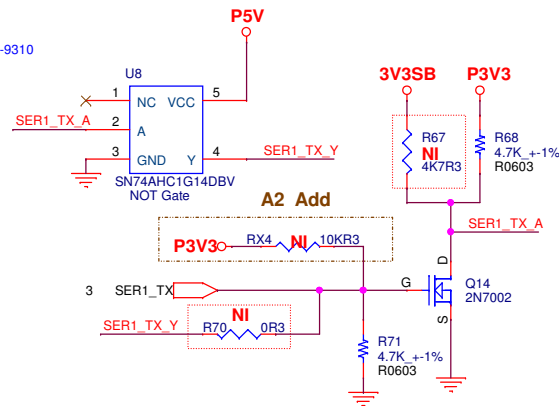
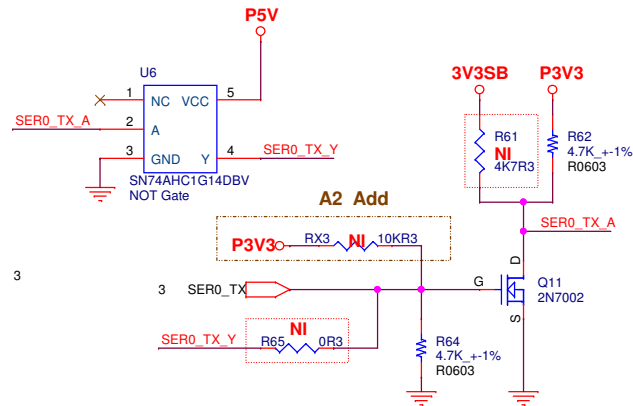
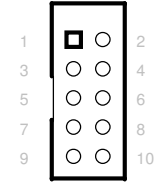
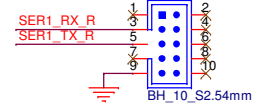
Q11,Q12,Q13,Q14 change P/N from 84-07002-0310 to 84-07002-9310



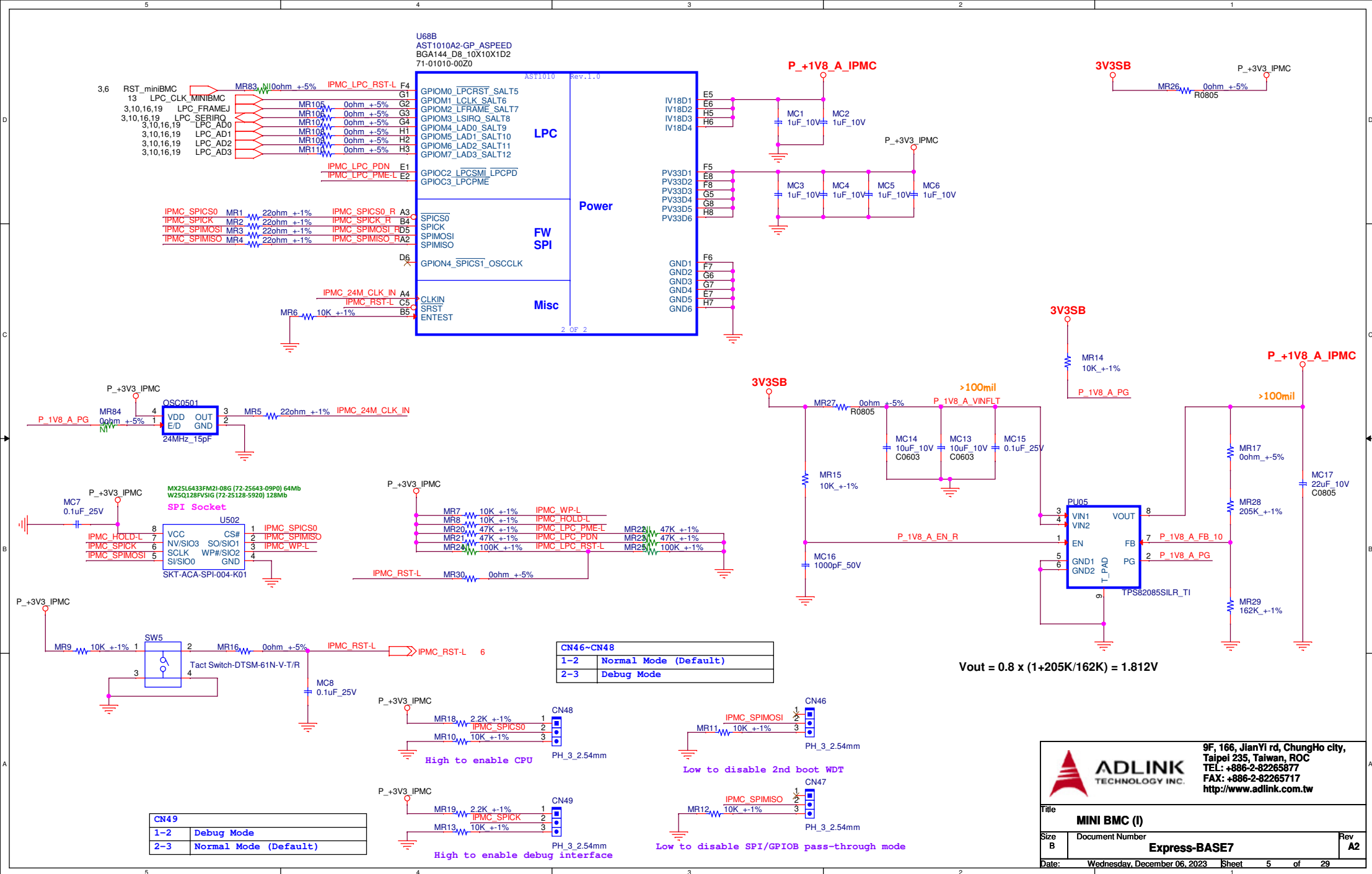
Port 1



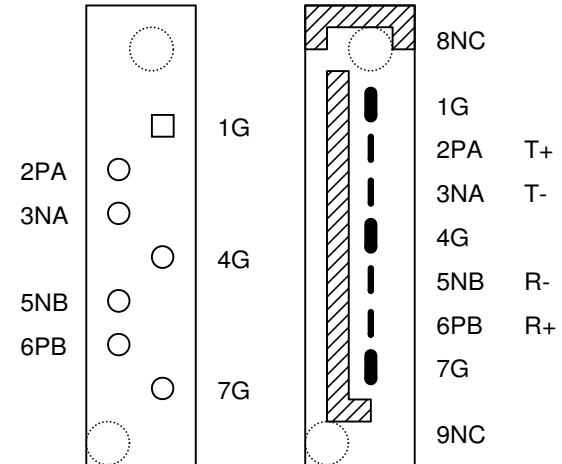
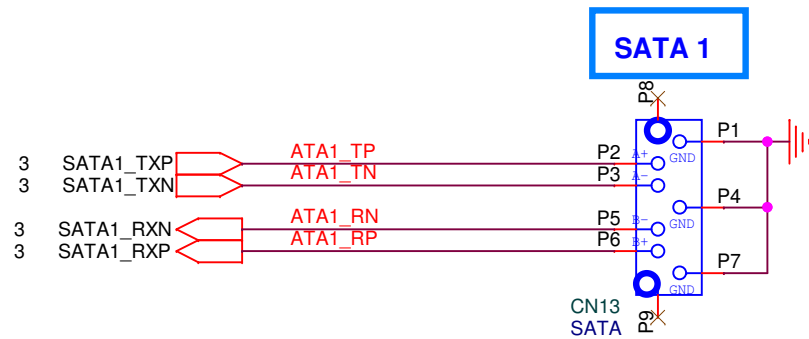
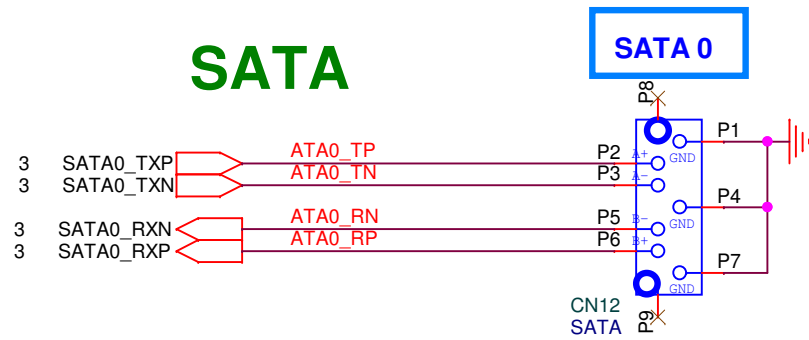
Port 2



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Title	Module series port		
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SATA



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Title

SATA

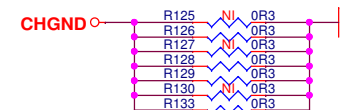
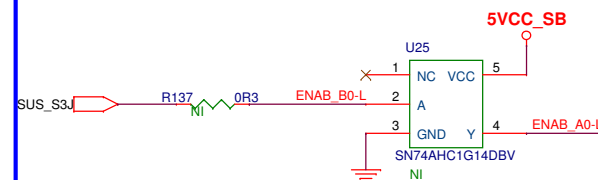
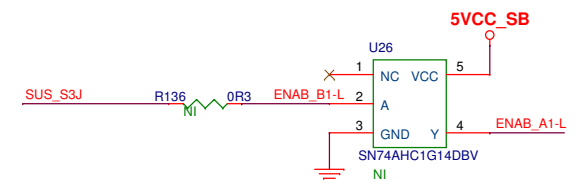
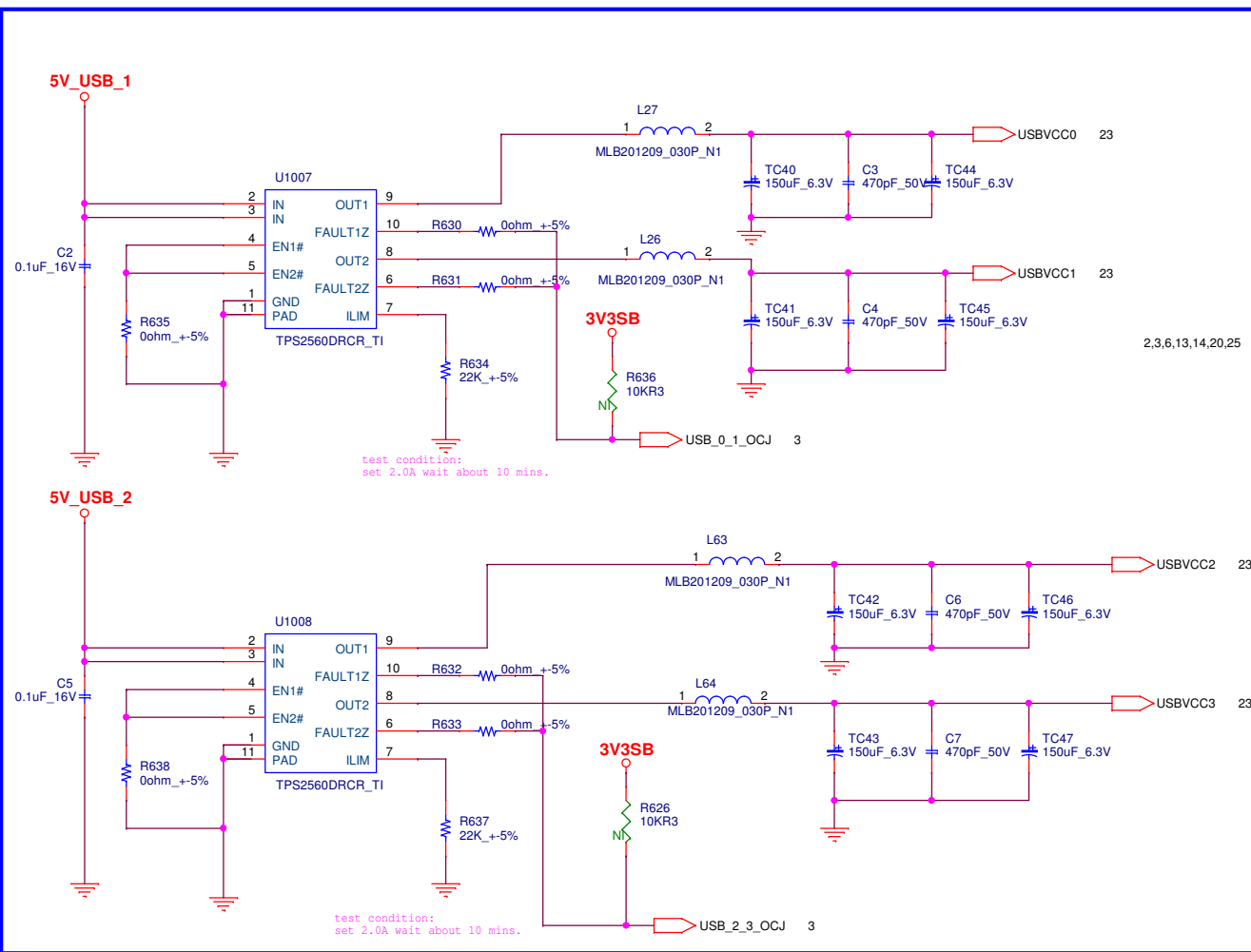
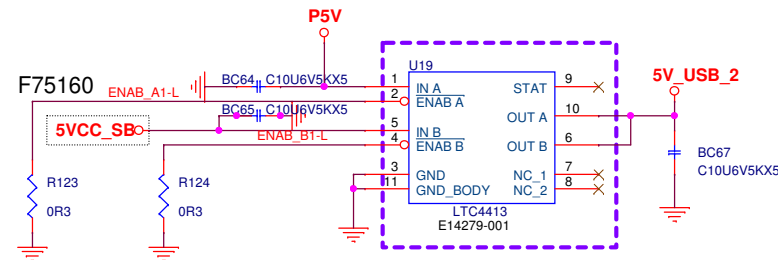
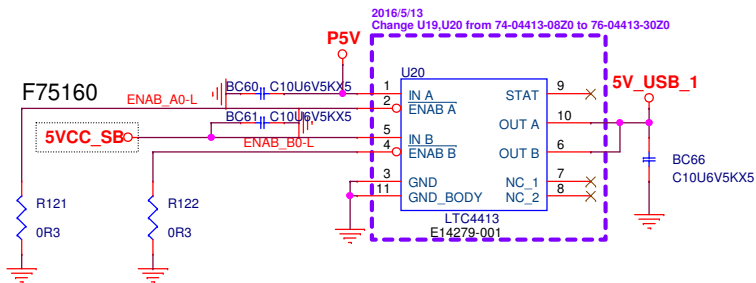
Size
A

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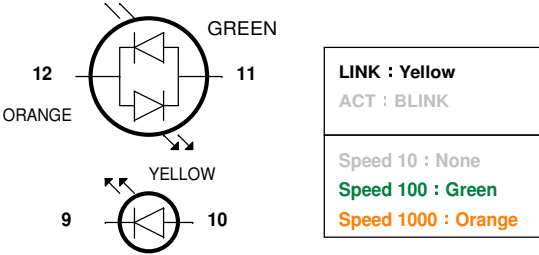
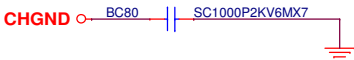
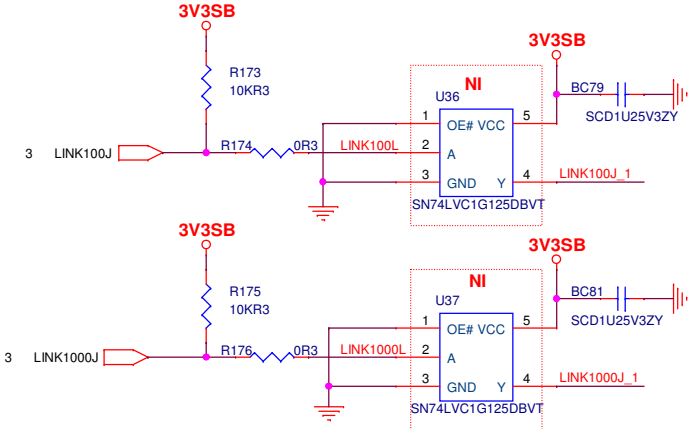
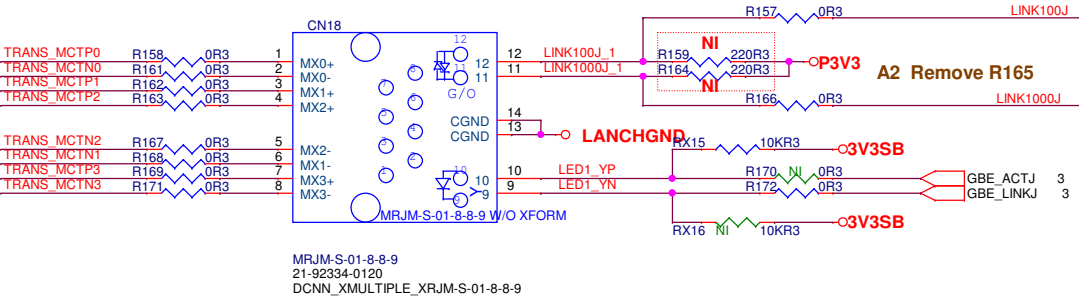
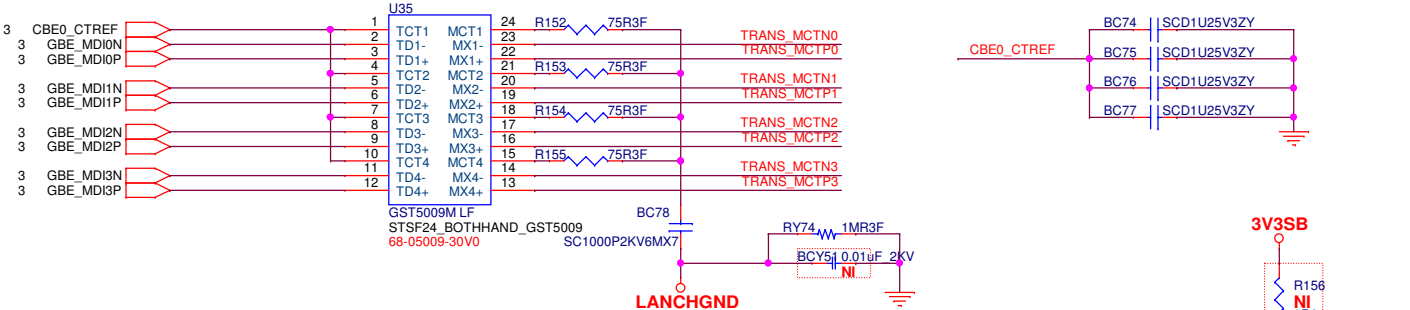
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A2 Change -
2016/09/13
Change R145,R147 to 64-64915-4490
2016/10/04
Change OC# schematic

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Title USB 2.0 / USB3.0			
Size B	Document Number Express-BASE7		Rev A2
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Giga LAN

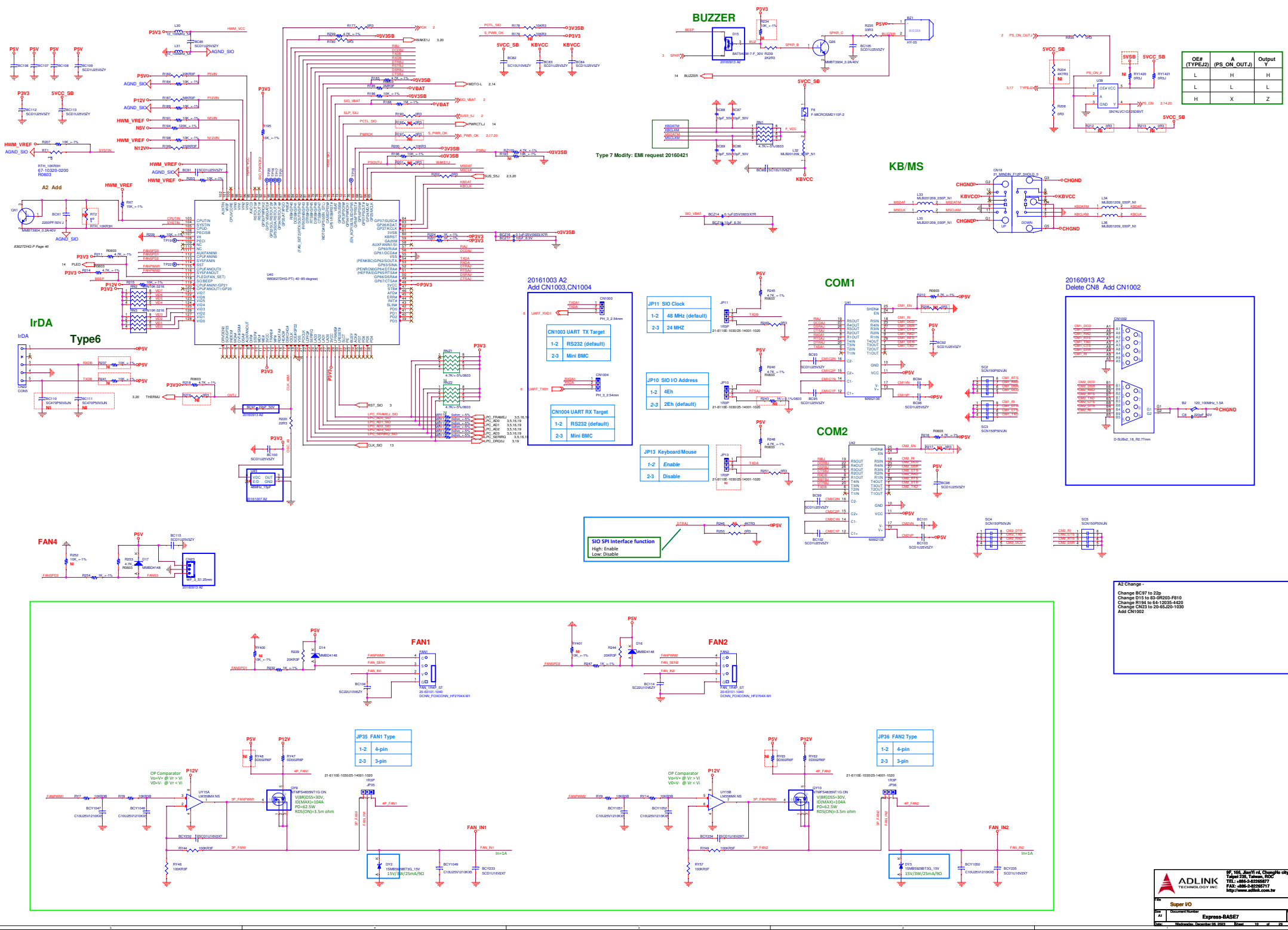


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DEF (TYPE2)	A (PS_ON_OUT)	Output
L	H	H
L	L	L
H	X	Z

20161003 A2
Add CN1003, CN1004

CN1003 UART TX Target
1-2 RS232 (default)
2-3 Mini BMC

CN1004 UART RX Target
1-2 RS232 (default)
2-3 Mini BMC

20160913 A2
Delete CN8 Add CN1002

A2 Change -
Change BC87 to 22p
Change D15 to 05-09205-F810
Change R184 to 64-12035-4420
Change CN82 to 59-05-025-1030
Add CN1002

SIO SPI Interface function
High: Enable
Low: Disable

JP11 SIO Clock

1-2 48 MHz (default)
2-3 24 MHz

JP10 SIO I/O Address

1-2 4Eh
2-3 2Eh (default)

JP13 Keyboard/Mouse

1-2 Enable
2-3 Disable

COM1

COM2

FAN1

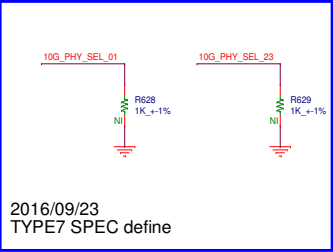
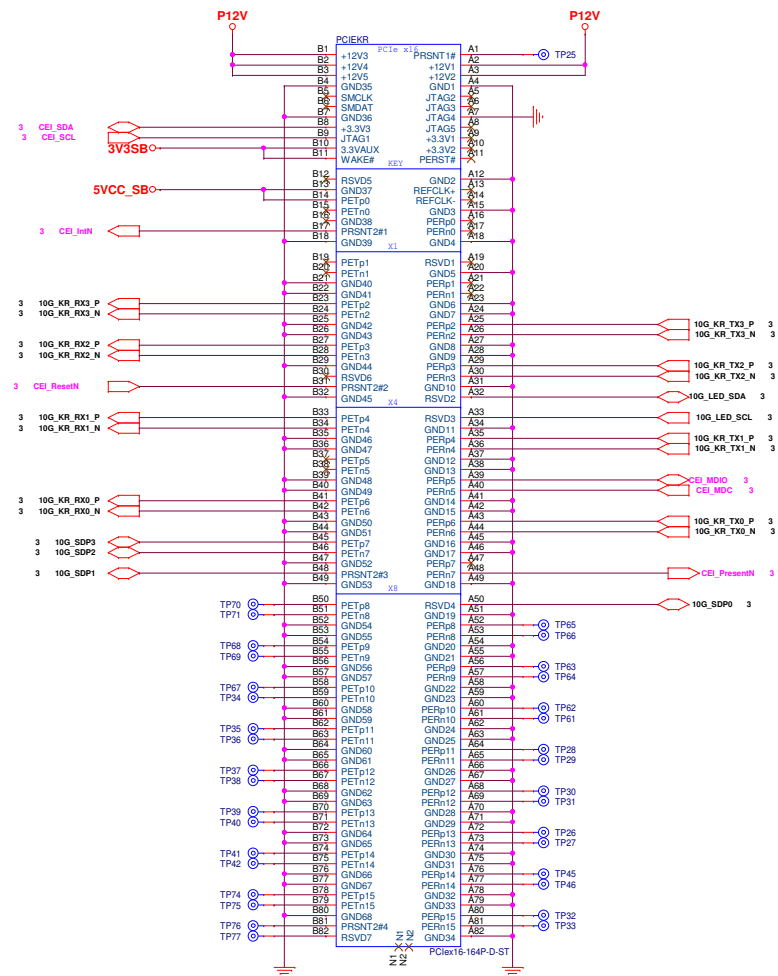
FAN2

FAN3

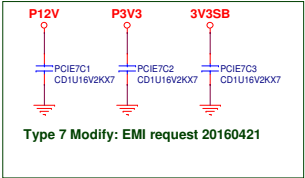
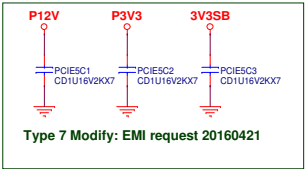
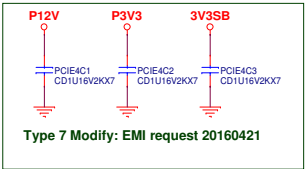
FAN4

If customer would like to use ATX power for CEI card design, please contact ADLINK

Type 7 Modify

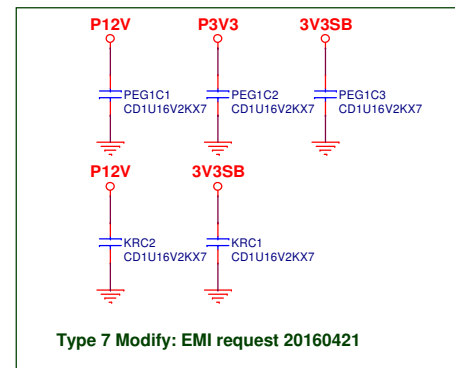
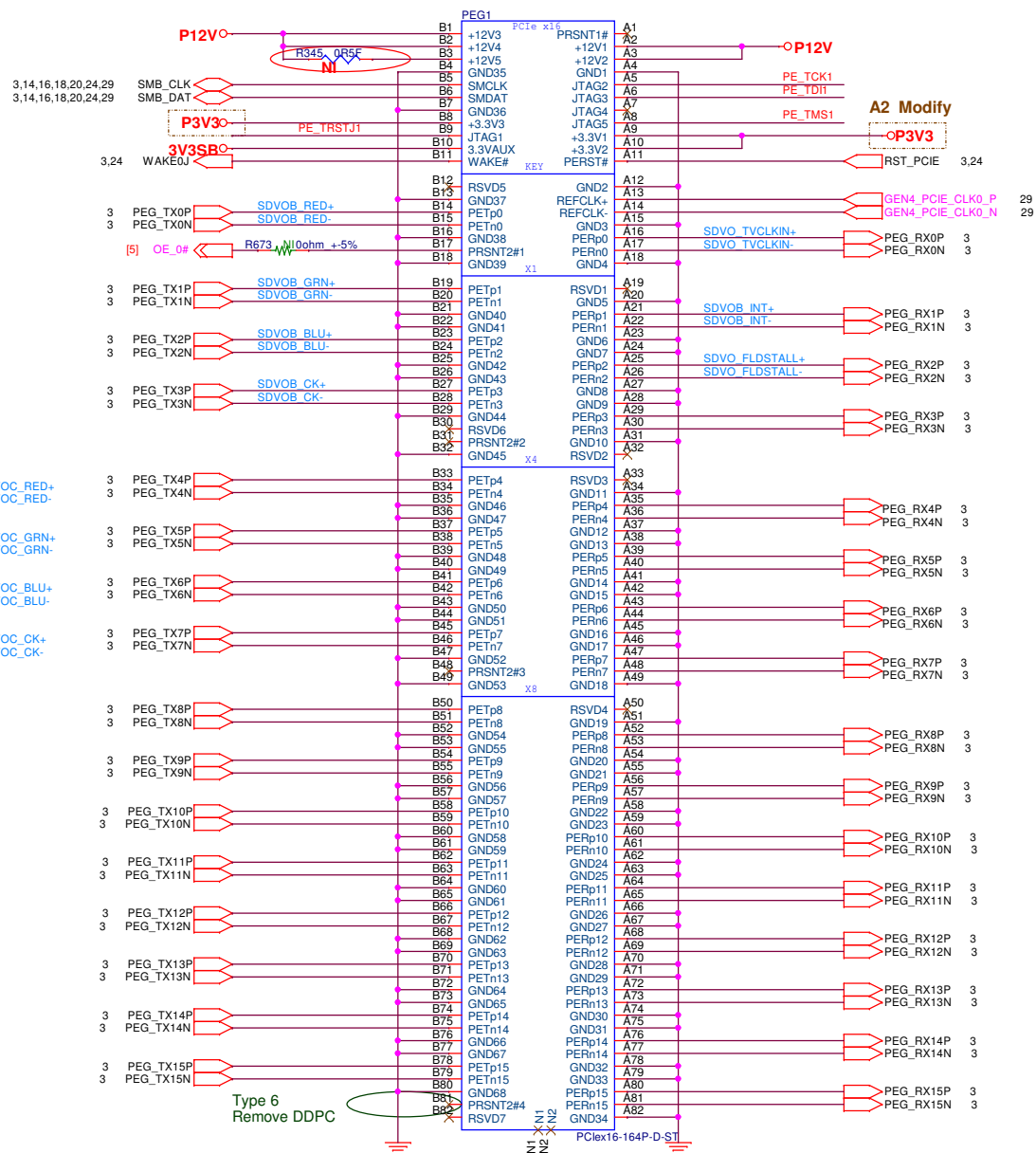


2016/09/23
TYPE7 SPEC define



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Type 7 Modify: EMI request 20160421

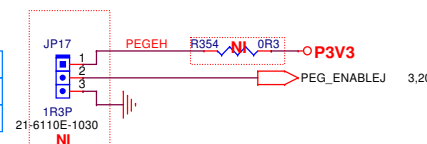
Power Supply Rail Requirements

Power Rail	x1 Connector	x16 Connector
+3.3V		
Voltage tolerance	9%	9%
Supply Current	3.0 A	3.0 A
Capacitive Load	1000 uF	1000 uF
+12V		
Voltage tolerance	8%	8%
Supply Current	0.5 A	4.4 A
Capacitive Load	300 uF	2000 uF
+3.3Vaux		
Voltage tolerance	9%	9%
Supply Current		
Wakeup Enabled	375 mA	375 mA
Non-wakeup Enabled	20 mA	20 mA
Capacitive Load	150 uF	150 uF
	25 W	60 W

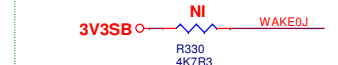
The power supply rails available at the PCI Express connectors, based on the number of PCI Express lanes supported by the connectors.

R353 PEG Reverse	
ON	Reverse
OFF	Standard

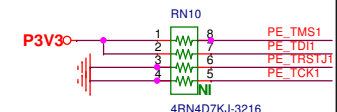
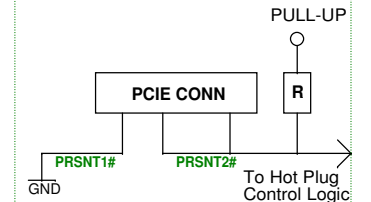
JP17 PEG Enable	
1-2	Disable
2-3	Enable



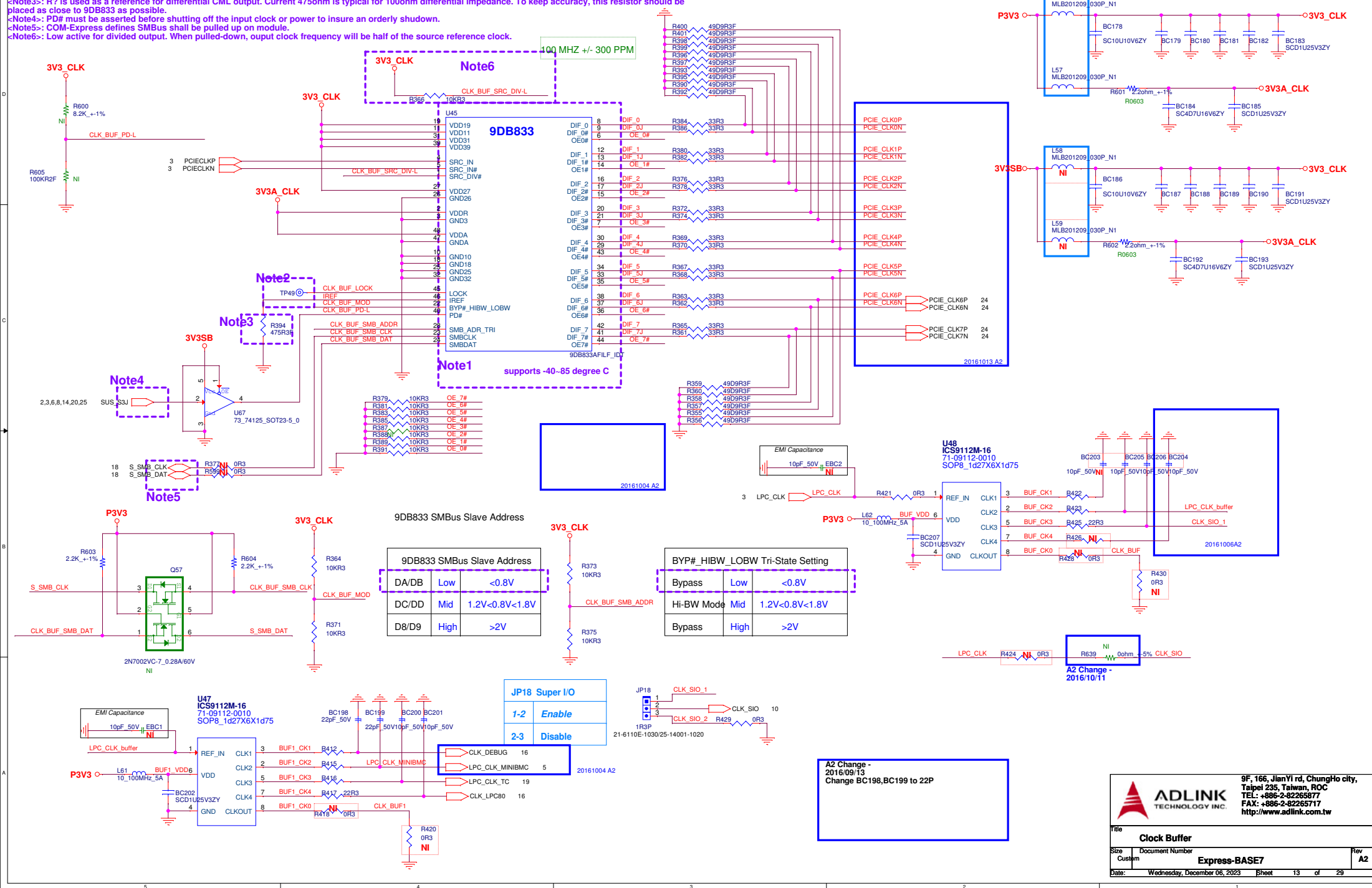
The WAKE# signal is an open drain, active low signal that is driven low by a PCI Express component to reactivate the PCI Express slot's main power rails and reference clocks.



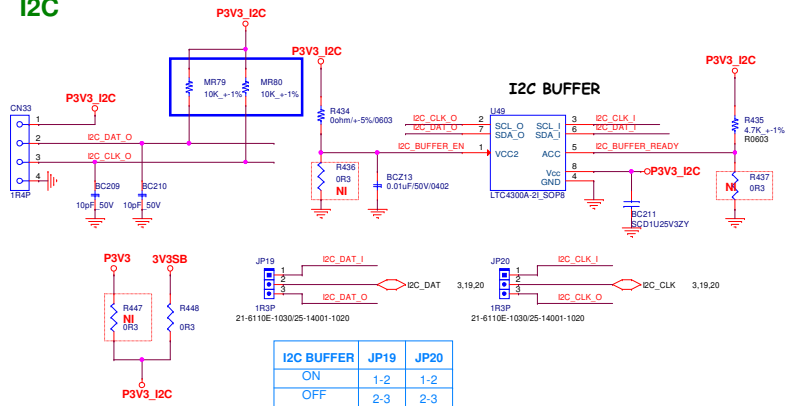
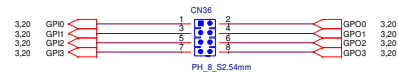
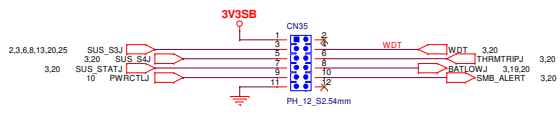
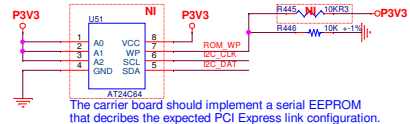
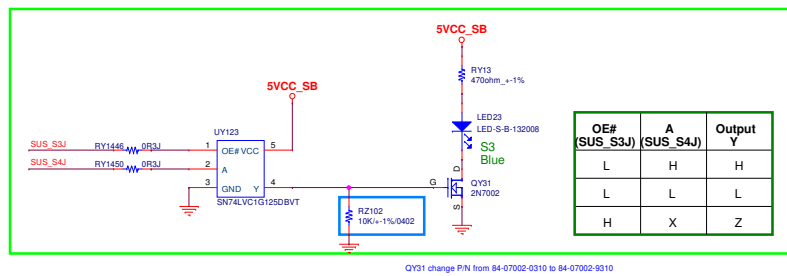
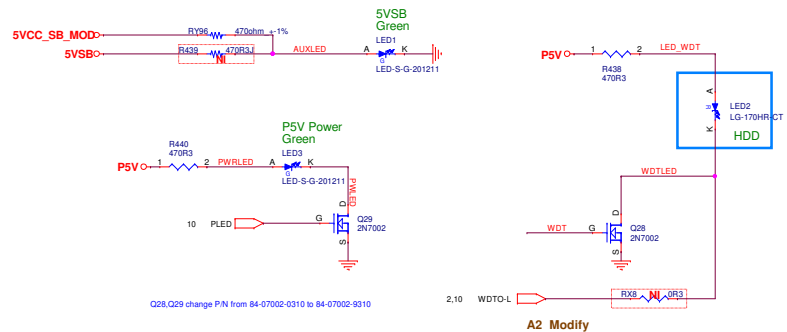
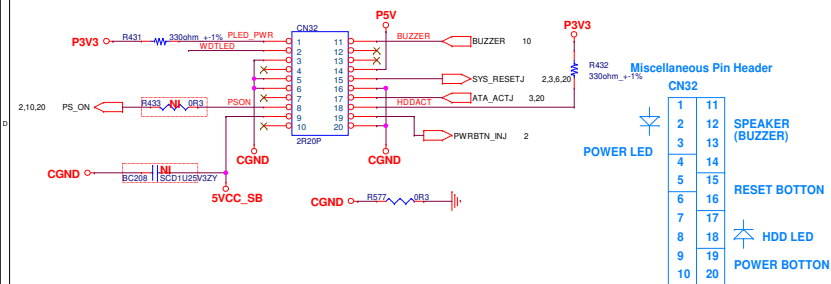
PCI Express Hot-Plug controller detects



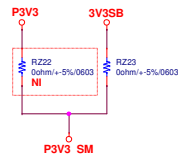
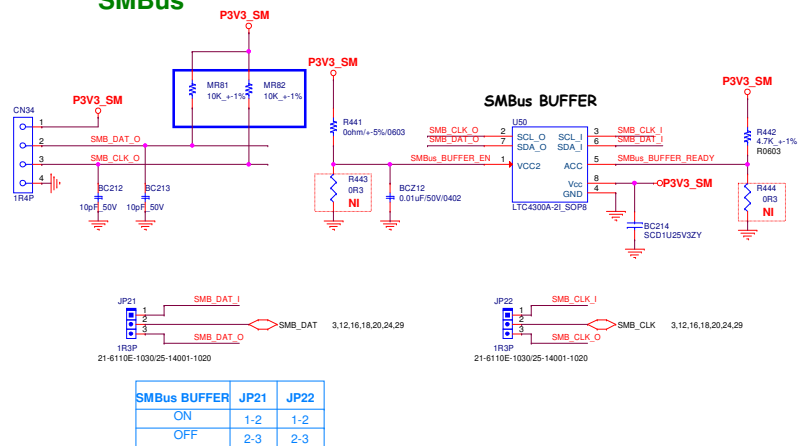
<Note1>: To support PCIe Gen3, phase jitter shall < 1.0ps(rms) and 9DB833 is used in order to support PCIe Gen3.
 <Note2>: A 3.3V output from LOCK indicates PLL's lock is achieved.
 <Note3>: R7 is used as a reference for differential CML output. Current 475ohm is typical for 100ohm differential impedance. To keep accuracy, this resistor should be placed as close to 9DB833 as possible.
 <Note4>: PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown.
 <Note5>: COM-Express defines SMBus shall be pulled up on module.
 <Note6>: Low active for divided output. When pulled-down, output clock frequency will be half of the source reference clock.



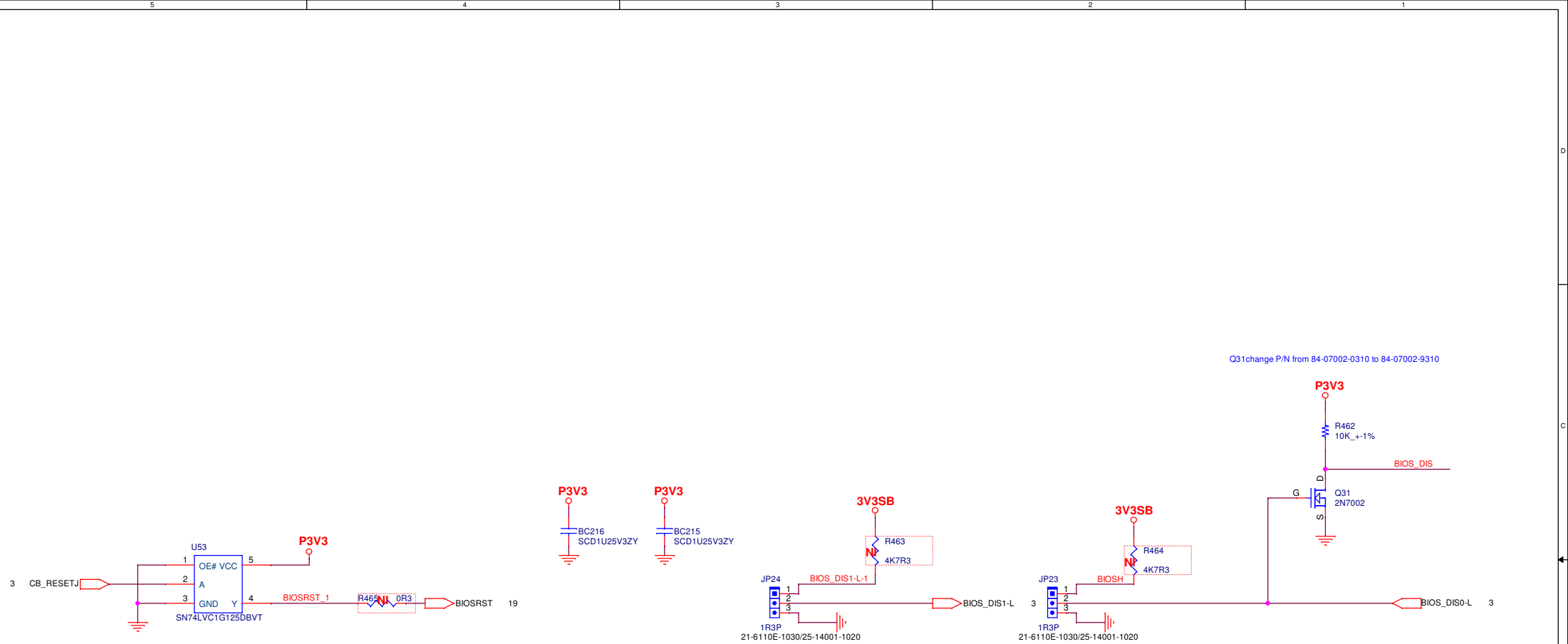
Misc.



SMBus

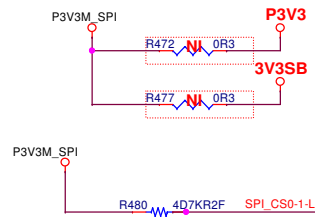
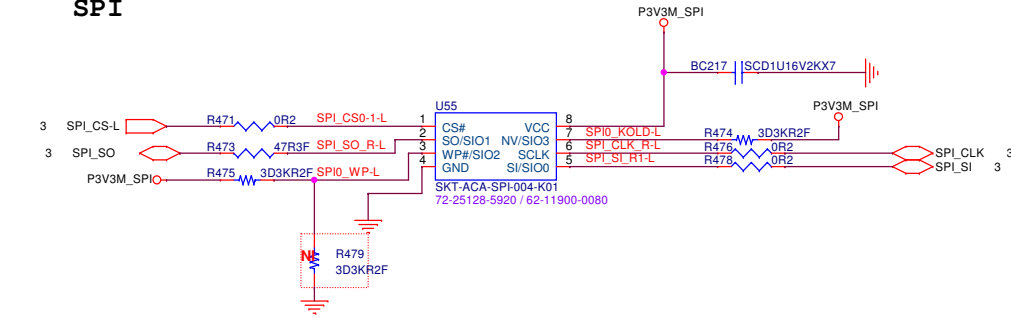


A2 Change -



JP23 (BIOS_DIS0#)	JP24 (BIOS_DIS1#)	BIOS Boot Device Select
1 - 2	1 - 2	Module SPI0 / SPI1
2 - 3	1 - 2	FWH on Carrier (on longer supported)
1 - 2	2 - 3	Module SPI0 / Carrier SPI1
2 - 3	2 - 3	Carrier SPI0 / Module SPI1

SPI



A3 Change -

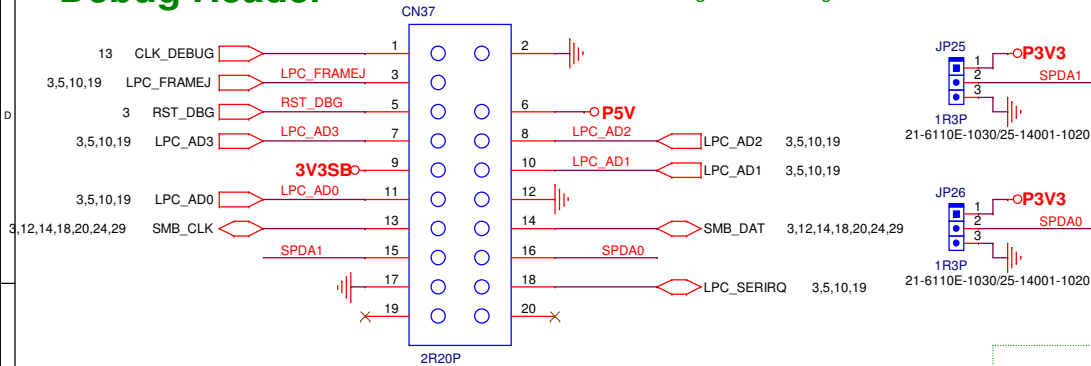


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Title External BIOS& SPI connector		
Size A3	Document Number Express-BASE7	Rev A2
Date: Wednesday, December 06, 2023 Sheet 15 of 29		

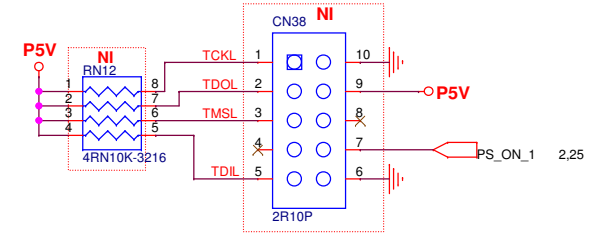
Debug Header

Reference Spec.
Installable LPC Debug Module Design Guide

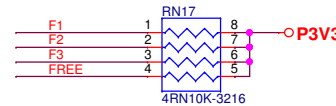
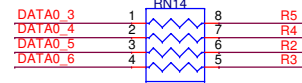
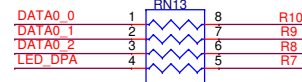
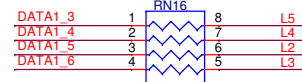
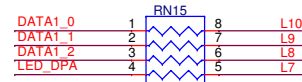
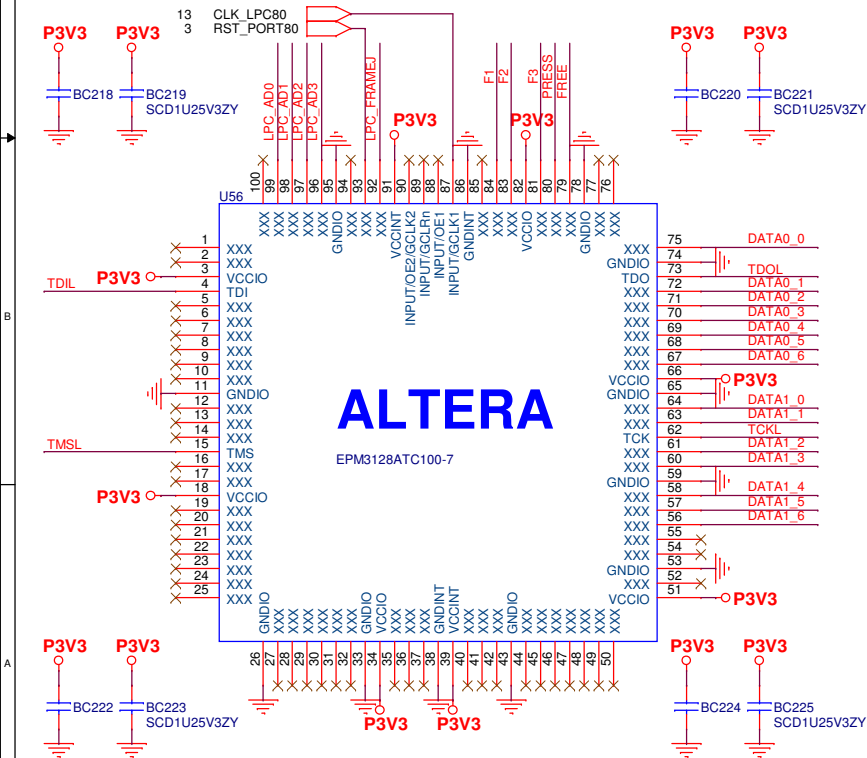


JP25 EEPROM A1	
1-2	High
2-3	Low

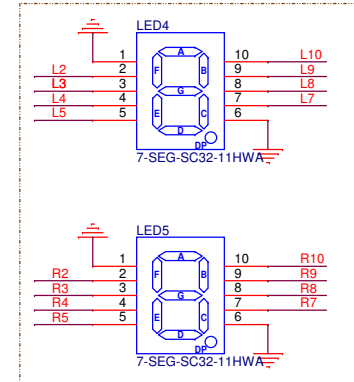
JP26 EEPROM A0	
1-2	High
2-3	Low



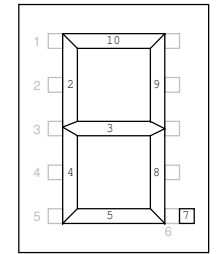
LPC Debug Port



A2 Modify



7-SEG LED (Top View)



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Title
LPC Debug Module

Size
B

Document Number
Express-BASE7

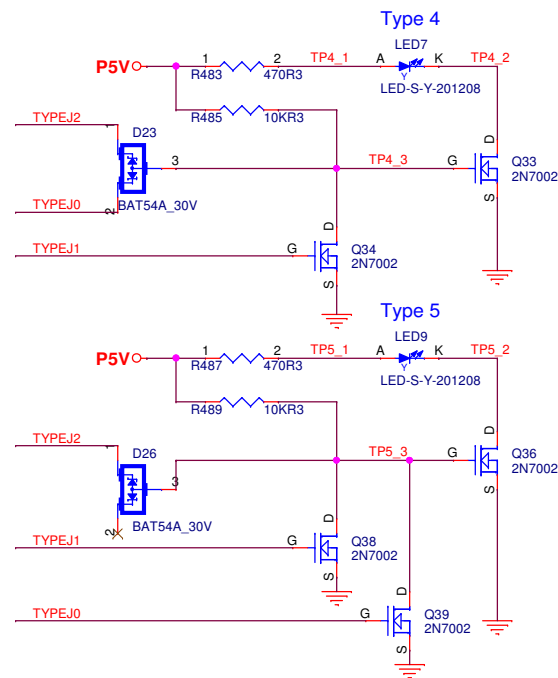
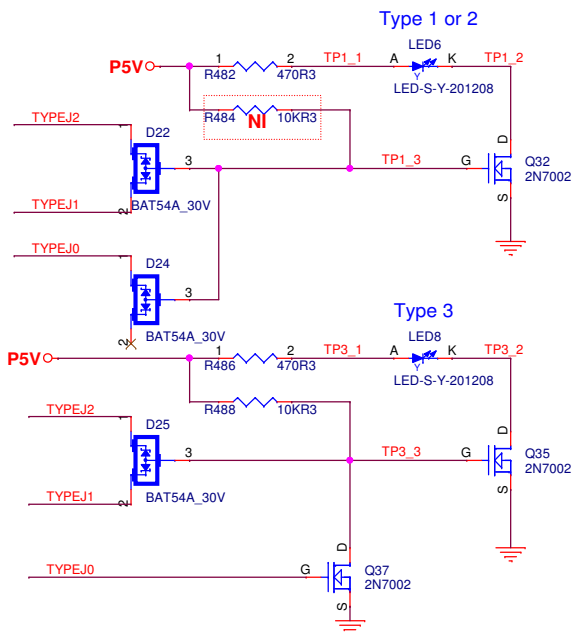
Date:
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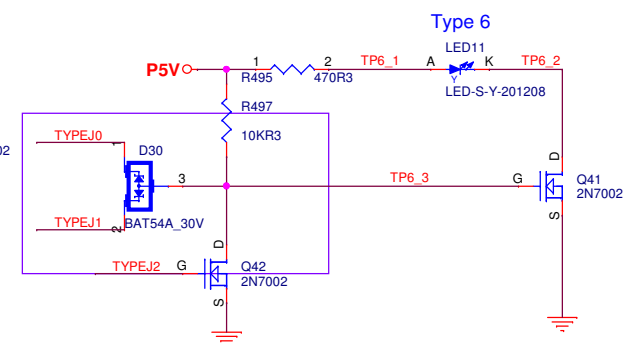
Rev
A2

Module Pin-out Type LEDs

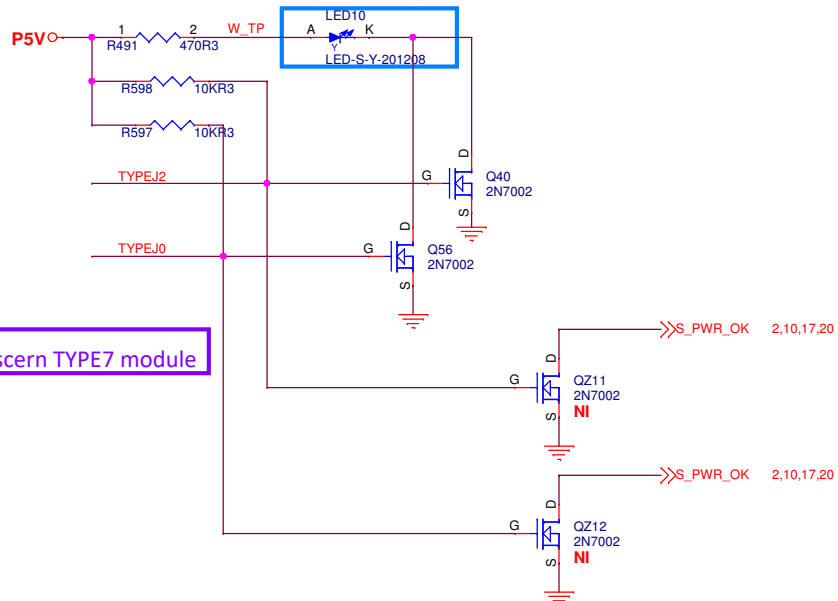
Q32,Q33,Q34,Q35,Q36,Q37,Q38,Q39,Q40,Q41,Q42,Q53,Q54,Q55,Q56 change P/N from 84-07002-0310 to 84-07002-9310



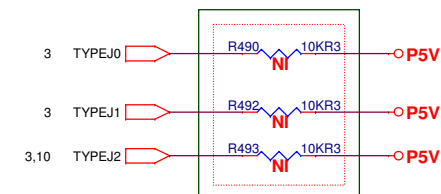
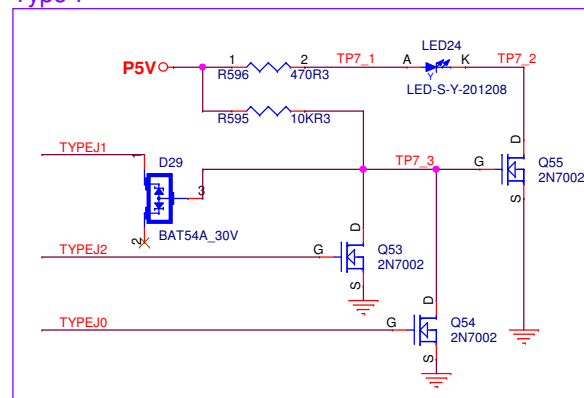
Module	TYPE2#	TYPE1#	TYPE0#
Type 1	X	X	X
Type 2	N C	N C	N C
Type 3	N C	N C	GND
Type 4	N C	GND	N C
Type 5	N C	GND	GND
Type 6	GND	N C	N C
Type 7	GND	N C	GND



Wrong Pin-out Type



Type 7

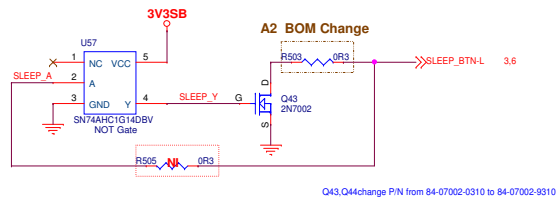
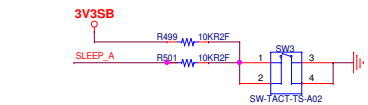


A3 Change -

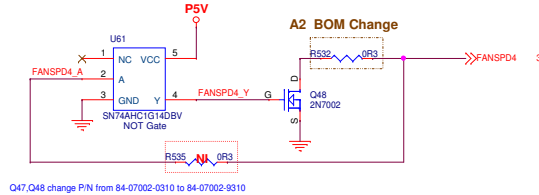
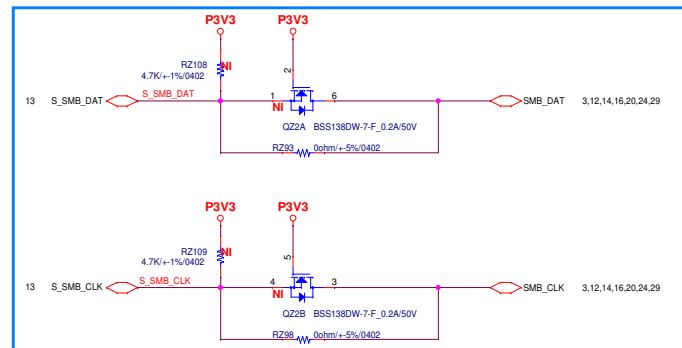
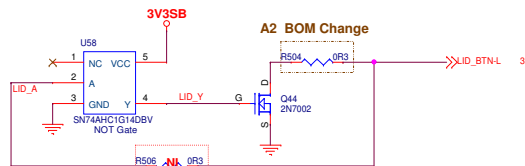
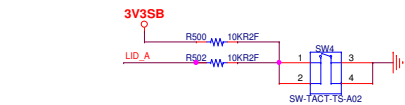
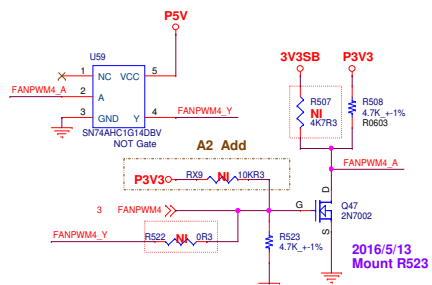
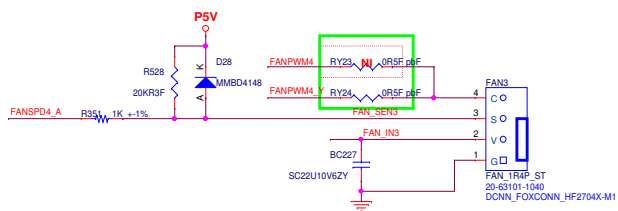
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Title	Pin-out Type LEDs		
Size B	Document Number	Express-BASE7	Rev A2
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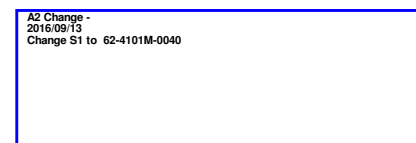
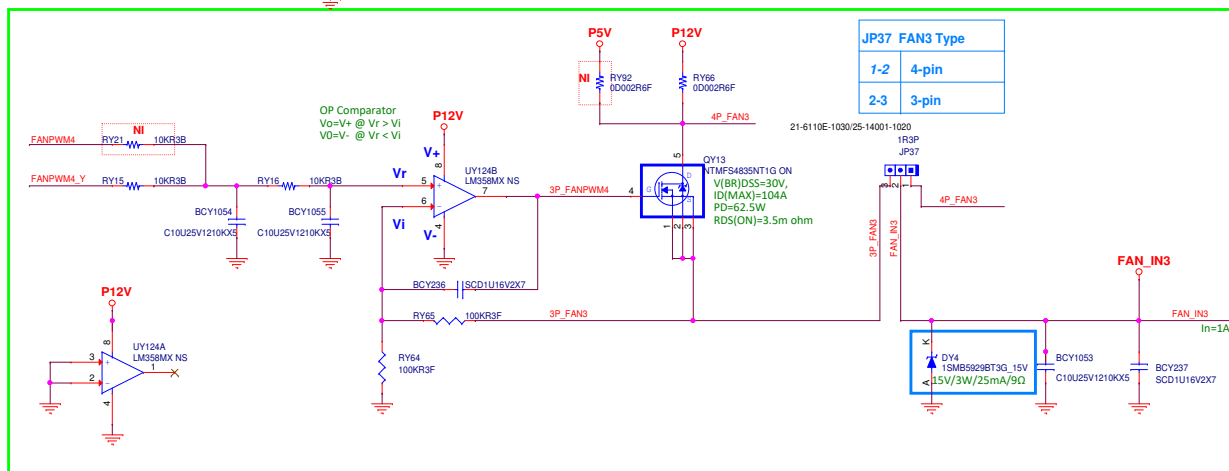
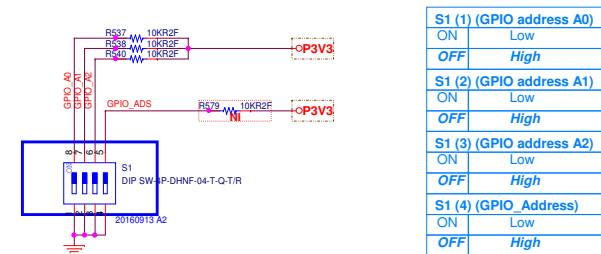
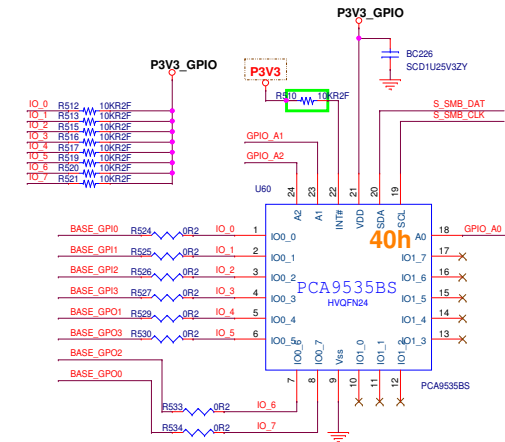
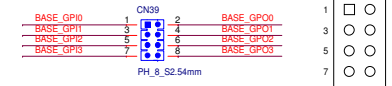
SLEEP BTN



FAN(from module)



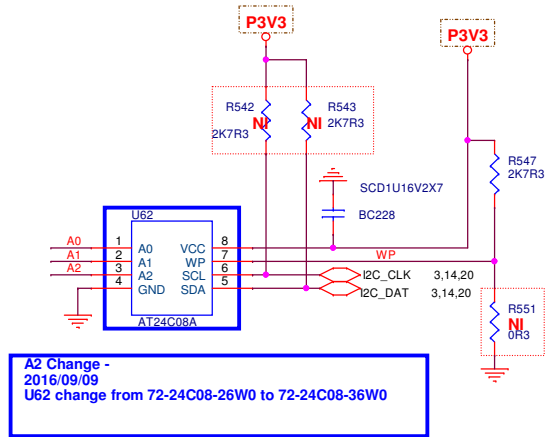
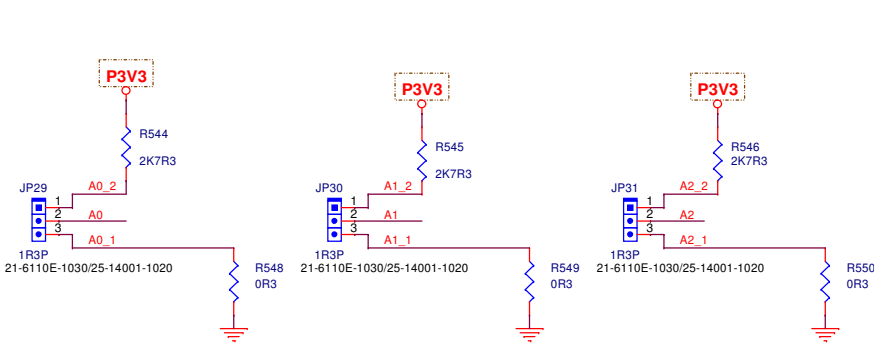
GPIO (base)



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Module FAN		
Size	Document Number	Rev
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I2C EEPROM

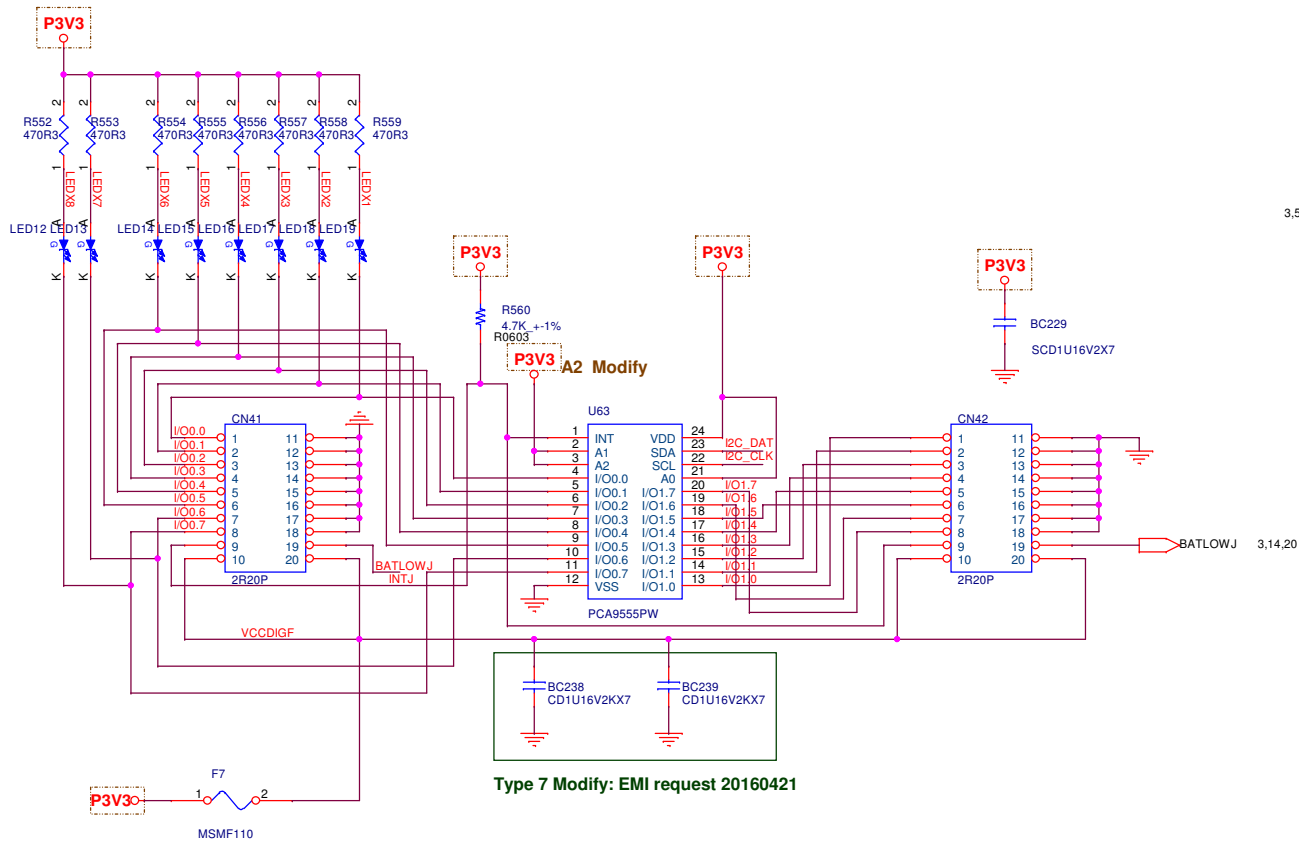


JP29 I2C EEPROM	
1-2	A0_High
2-3	A0_Low

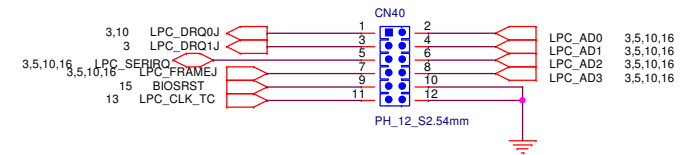
JP30 I2C EEPROM	
1-2	A1_High
2-3	A1_Low

JP31 I2C EEPROM	
1-2	A2_High
2-3	A2_Low

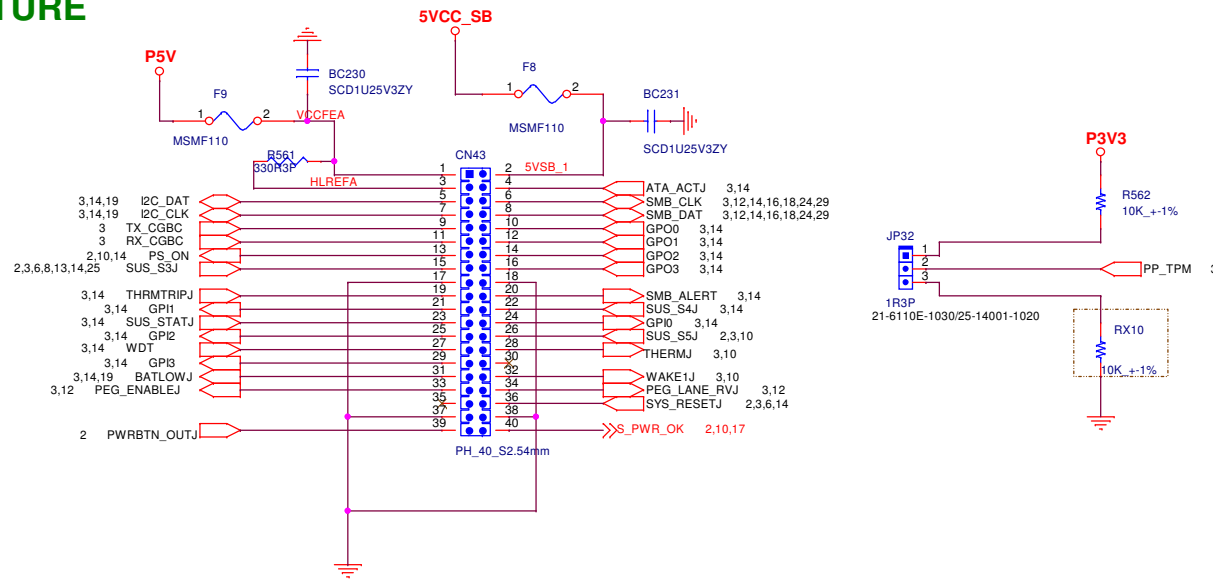
Digital IO



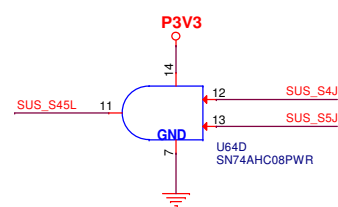
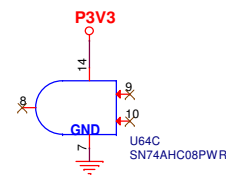
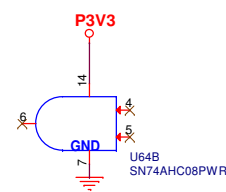
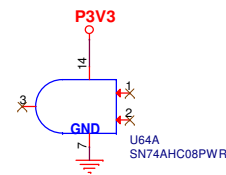
LPC Testconnector



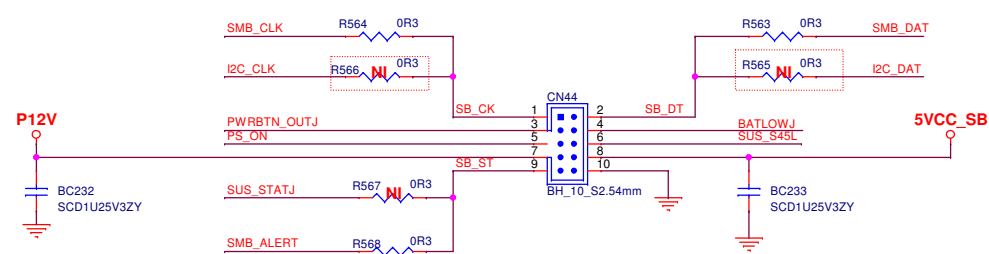
FEATURE



JP32 PP_TPM	
1-2	ON
2-3	OFF



Smart Battery



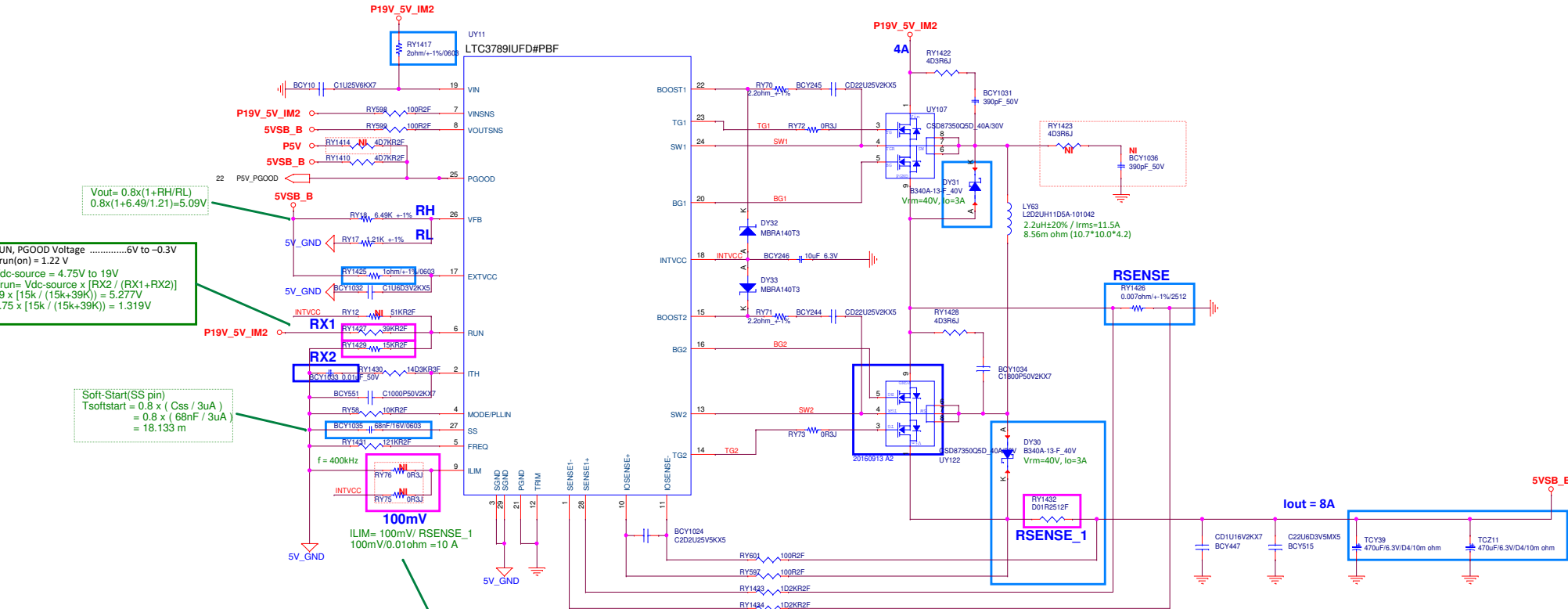


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Title		
FEATURE & TPM		
Size	Document Number	Rev
A3	Express-BASE7	A2
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P12V to P5V



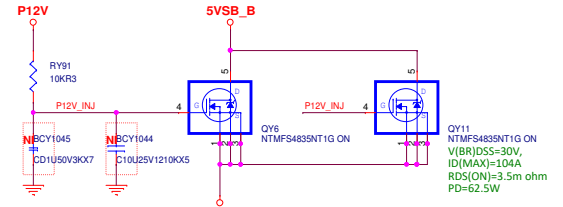
Run, PGOOD Voltage6V to -0.3V
Vrun(on) = 1.22 V
Vdc-source = 4.75V to 19V
Vrun= Vdc-source x [RX2 / (RX1+RX2)]
19 x [15k / (15k+39K)] = 5.277V
4.75 x [15k / (15k+39K)] = 1.319V

Soft-Start(SS pin)
Tsoftstart = 0.8 x (C_{ss} / 3uA)
= 0.8 x (68nF / 3uA)
= 18.133 ms

Programming Input/Output Current Limit
The input/output current limit is set by the ILIM pin for 50mV, 100mV or 140mV with ILIM pulled to the GND, floating, or tied to INTVCC, respectively.

Fault Conditions: Current Limit and Current Foldback
The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the boost region, maximum sense voltage and the sense resistance determine the maximum allowed inductor peak current, which is:
 $IL(MAX,BOOST) = 140mV / RSENSE$
In the buck region, maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current, which is:
 $IL(MAX,BUCK) = 90mV / RSENSE$

A2 Change -
2016/09/13
Change UY122 direction
Change LY68 to 68-20110-2080
Change RY17 to 64-12115-4490
Change RY18 to 64-64915-4490



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P19V_5V to P3V3

EN/PSV input Voltage: 2.2V to 5V
 $5 \times [30k / (10k + 30k)] = 3.75V$

$fsw = Vout / (Ton \times Vin)$
 $Rton = [(Ton - 10ns) \times Vin] / (25pF \times Vout)$

$VLDO = 750mV \times (1 + RLDO1 / RLDO2)$
 $0.75 \times (1 + 57.6k / 10k) = 5.07V$

ENL input Bias Voltage: -0.3 to Vin

The RILIM value is calculated by the following equation.
 $RILIM = 735 \times ILIM$
 $ILIM = 7.15k / 735$
 $= 9.727 A$

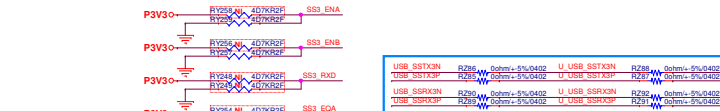
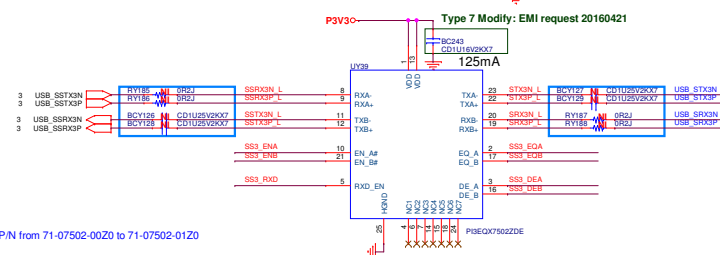
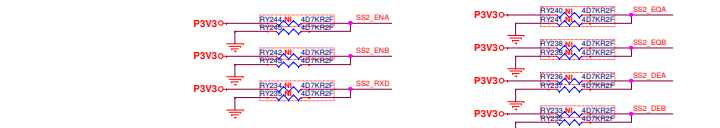
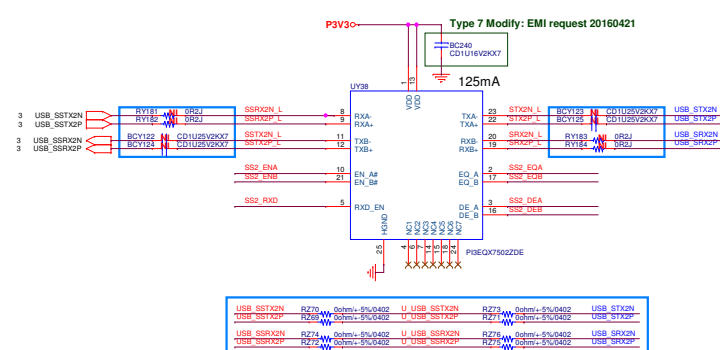
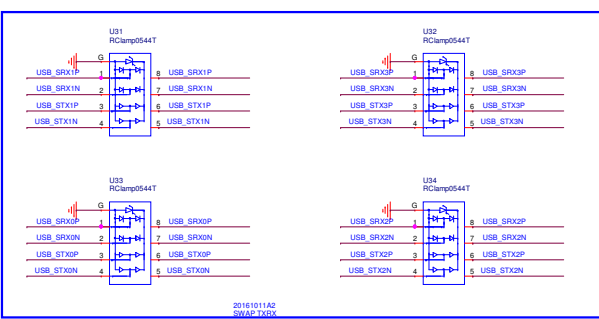
$Vout = 0.5 \times \{1 + (RX1 / RX2)\}$
 $= 0.5 \times \{1 + (5.6k / 1k)\}$
 $= 3.3$

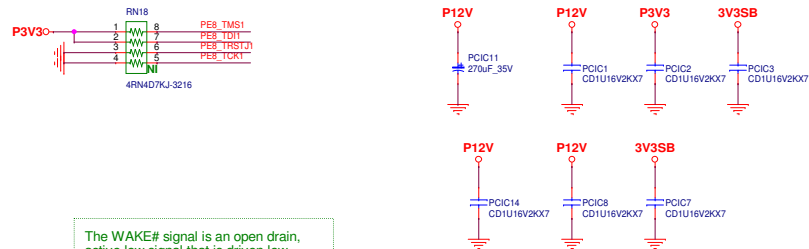
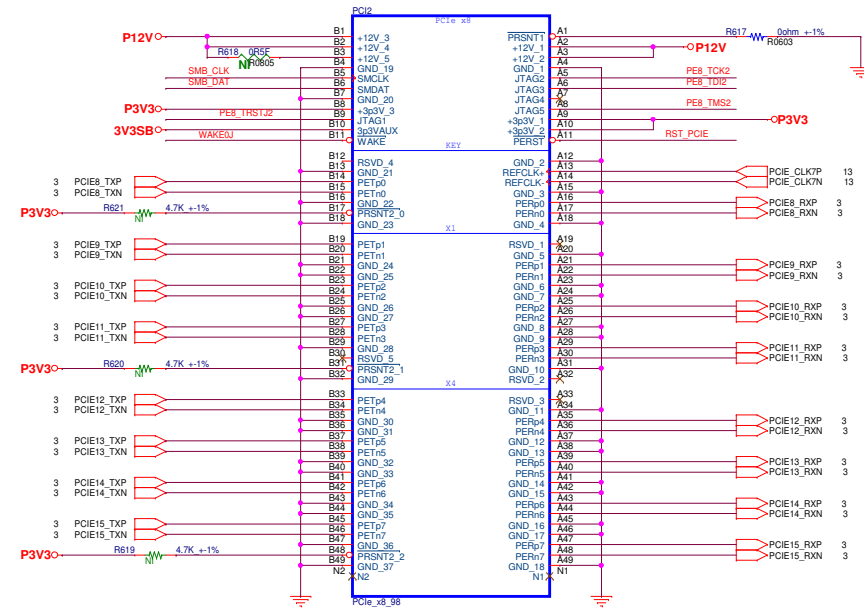
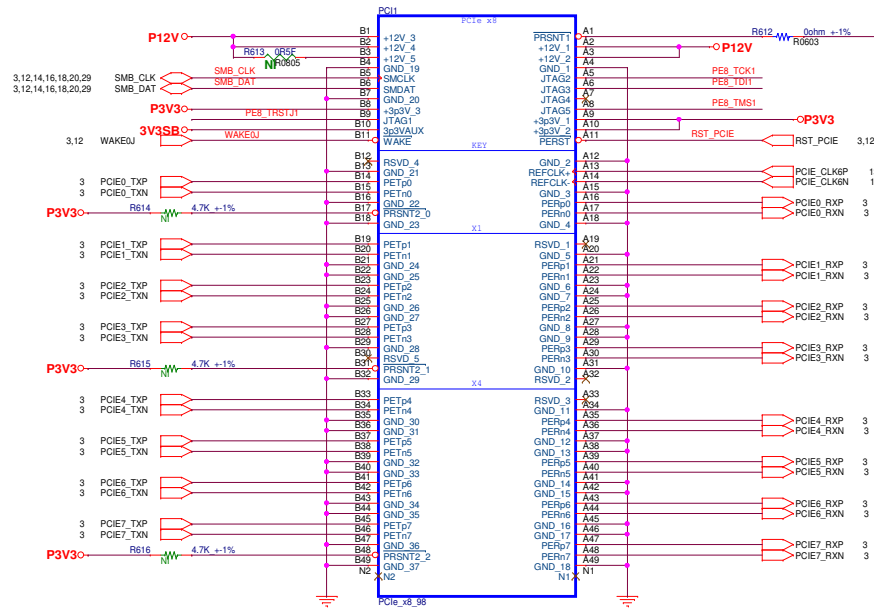
EN/PSV	ENL	LDO	Switcher
Disable	Low, <0.4V	OFF	OFF
Enable	Low, <0.4V	OFF	ON
Disable	1.0V < High < 2.6V	ON	OFF
Enable	1.0V < High < 2.6V	ON	OFF
Disable	High, >2.6V	ON	OFF
Enable	High, >2.6V	ON	ON

A3 Change -
2012/02/29
Change new power solution of P12V to P3V3
1. Remove U3(76-03728-50Z0)
2. Add UY120(76-00417-50Z0)(SC417)

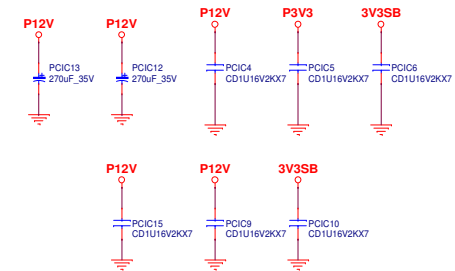
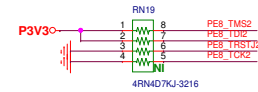
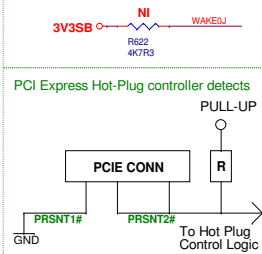
B1 Change -
2012/12/26
Power Solutions to fine turn
1. RY50 change from 10 ohm (64-10R05-4490)(0402) to 0 ohm(63-R0003-4510)(0603)
2013/01/03
1. BCY1017 Remove 100pF(78-10134-14A0)(0402)

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		Title P3V3	
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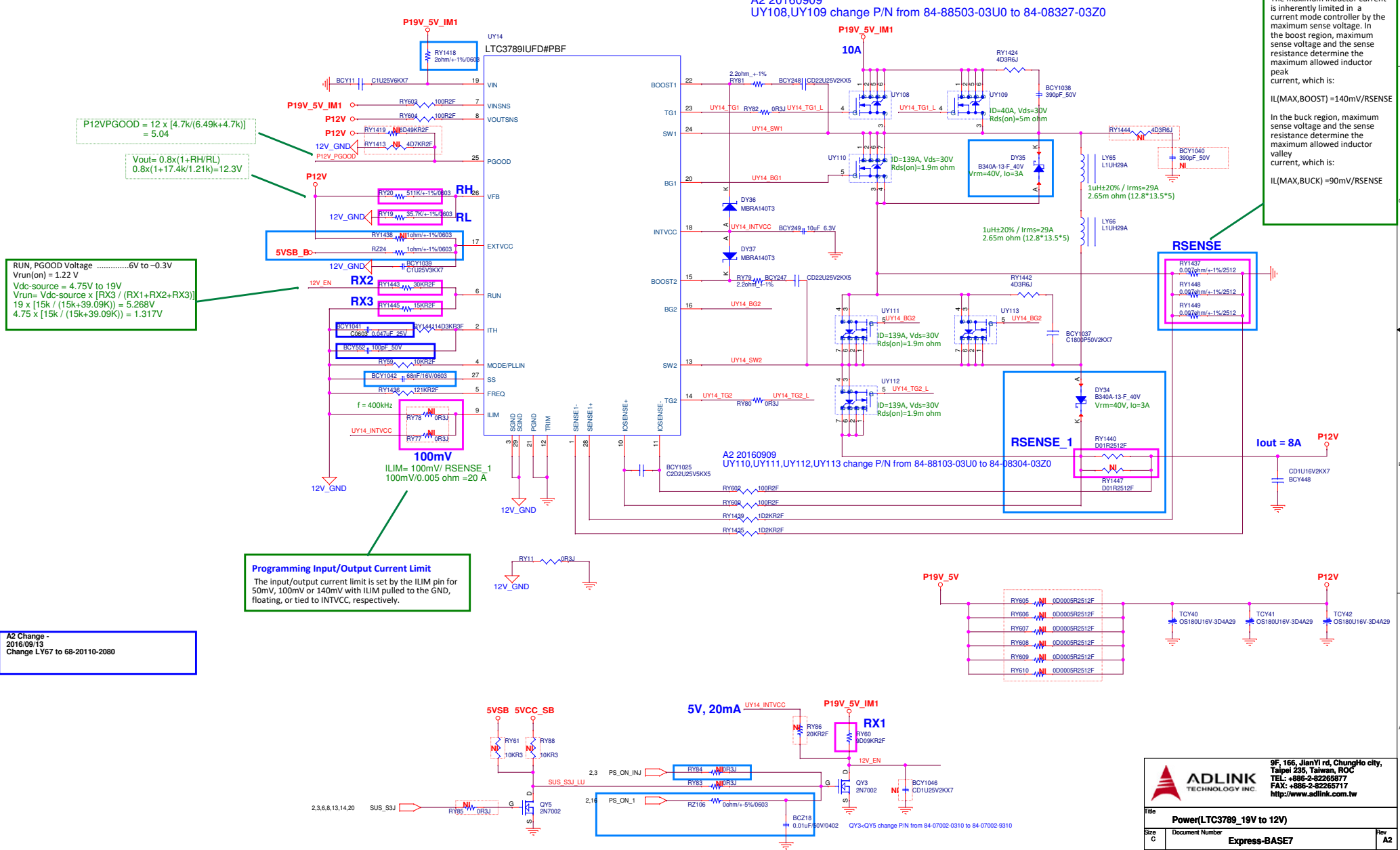




The WAKE# signal is an open drain, active low signal that is driven low by a PCI Express component to reactivate the PCI Express slot's main power rails and reference clocks.



P19V~P4V75 to P12V



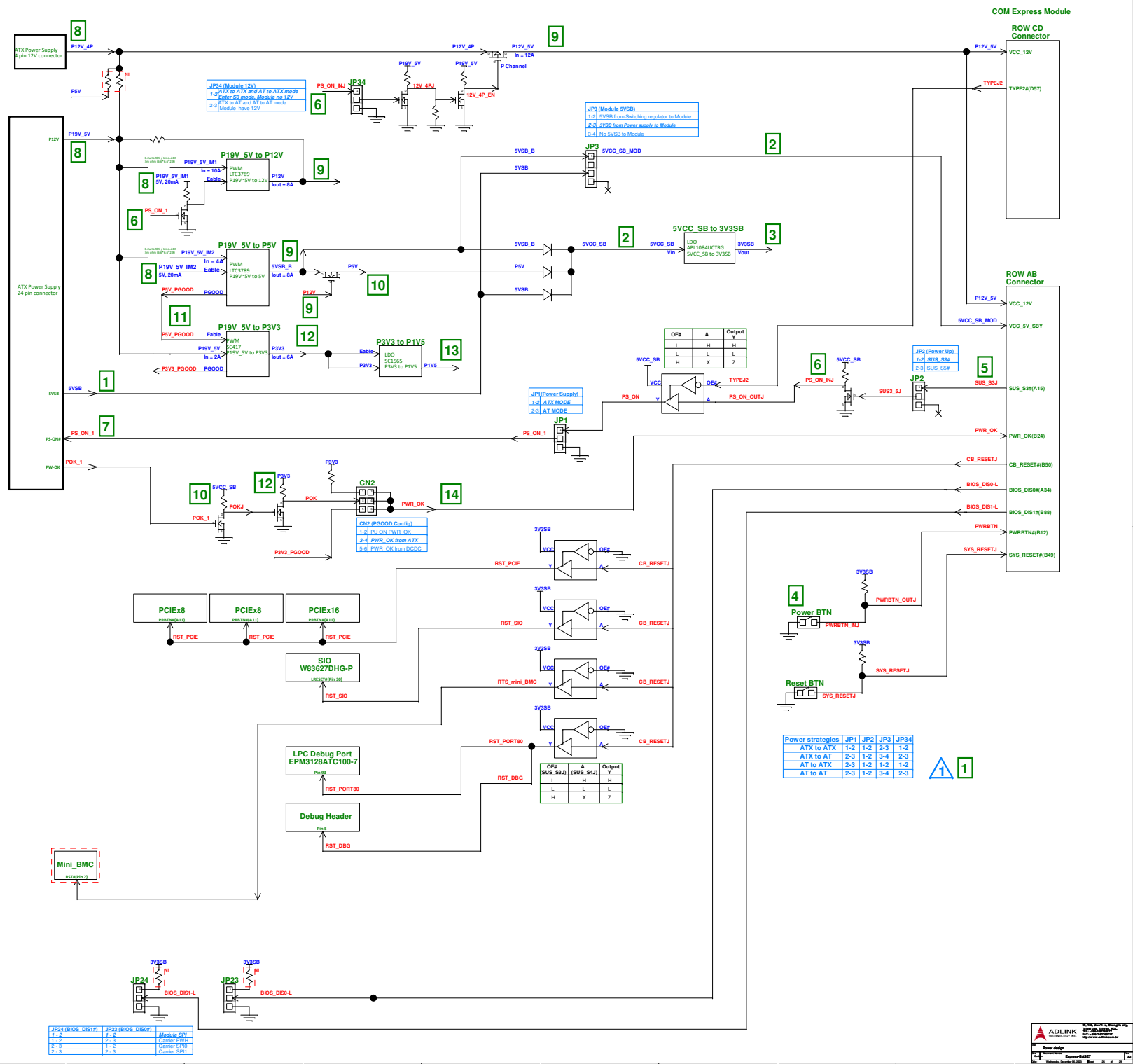
Fault Conditions: Current Limit and Current Foldback
The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the boost region, maximum sense voltage and the sense resistance determine the maximum allowed inductor peak current, which is:

$$I_L(\text{MAX_BOOST}) = 140\text{mV}/R_{\text{SENSE}}$$

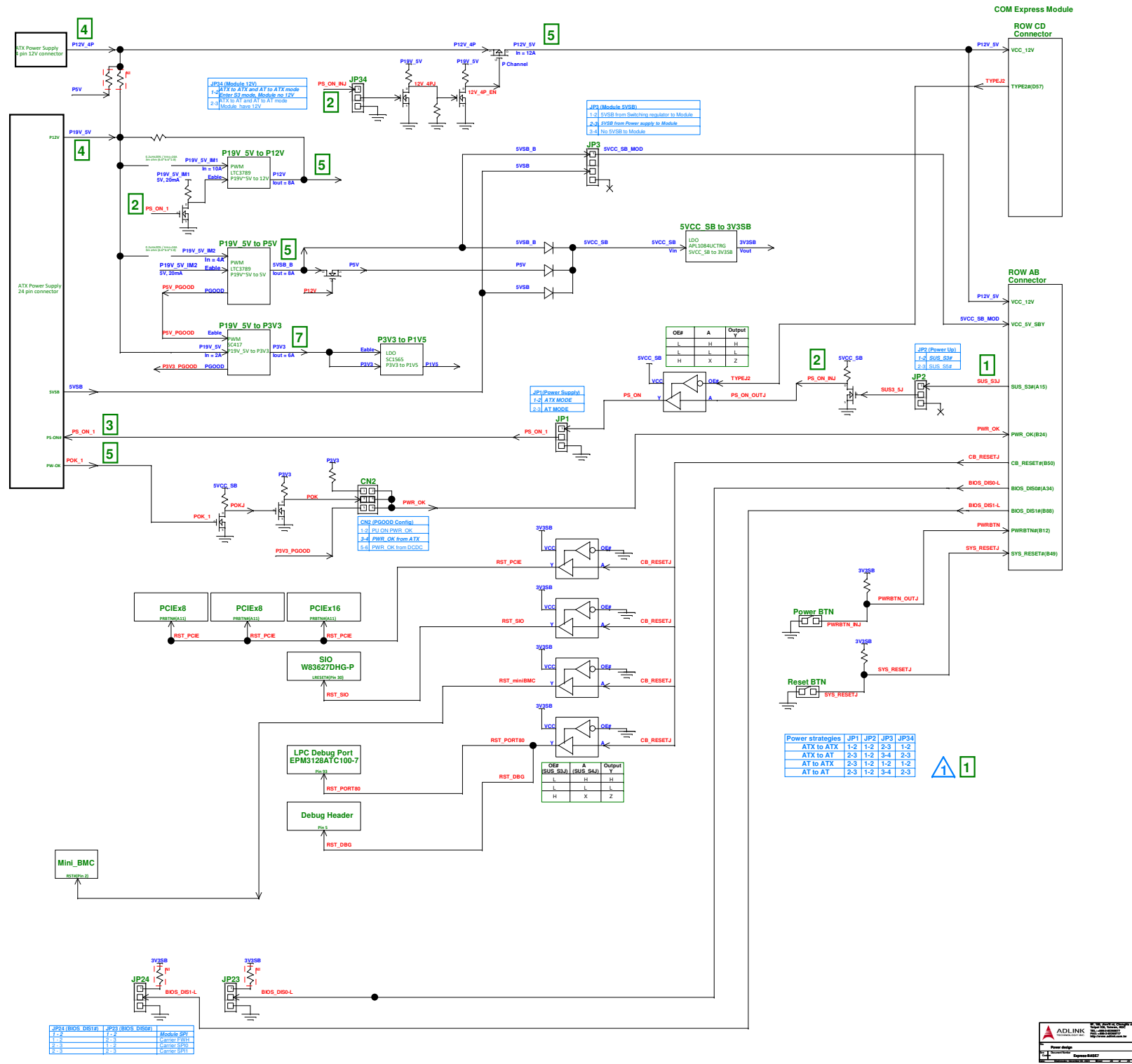
In the buck region, maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current, which is:

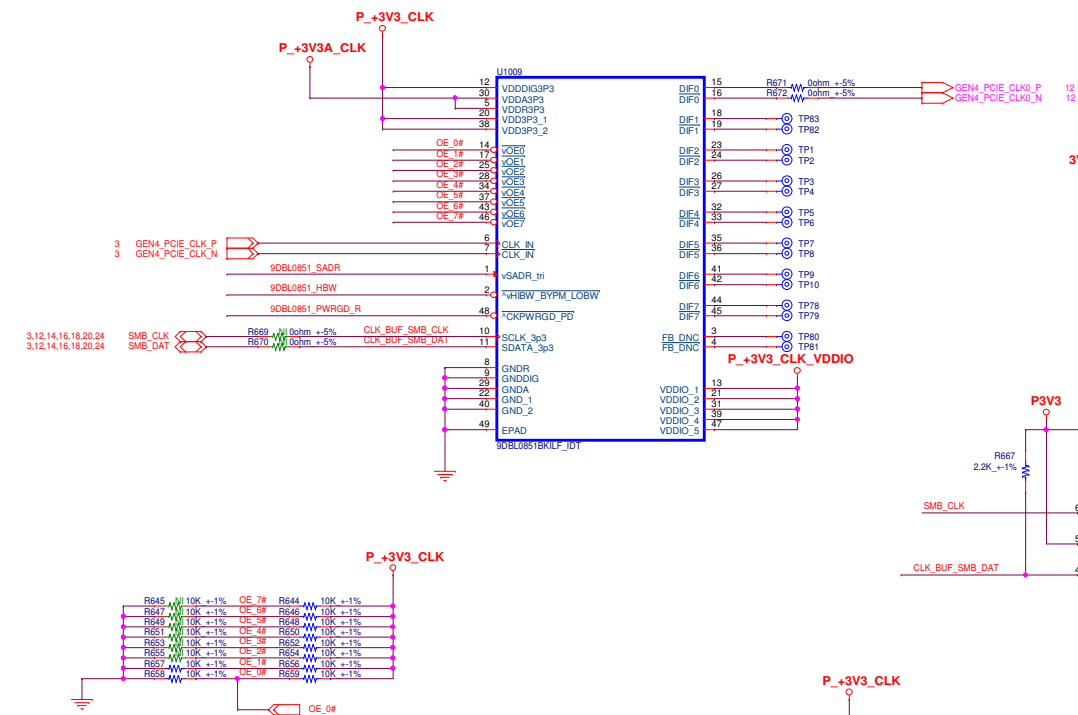
$$I_L(\text{MAX_BUCK}) = 90\text{mV}/R_{\text{SENSE}}$$

A2 Change -
2016/09/13
Change LY67 to 68-20110-2080









SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	X
	M	1101100	X
	1	1101101	X

Note: If not using CKPWRGD (CKPWRGD tied to VDD3.3), all 3.3V VDD need to transition from 2.1V to 3.135V in <300usec.

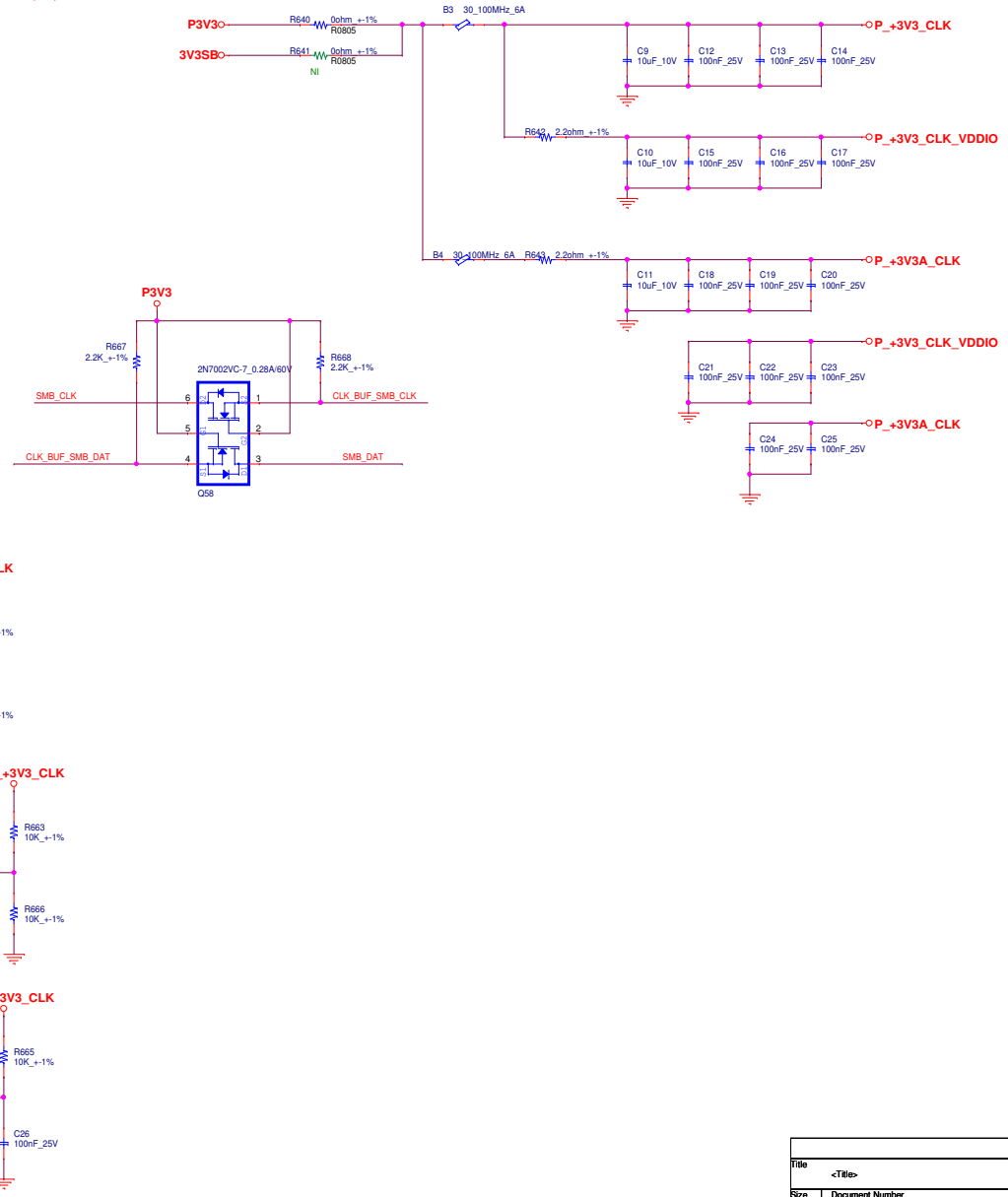
PLL Operating Mode

HIBW BypM LoBW#	MODE	Byte1 [7:6] Readback	Byte1 [4:3] Control
0	PLL Lo BW	00	00
M	Bypass	01	01
1	PLL HI BW	11	11

Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# P in	DIFx		PLL
				True O/P	Comp. O/P	
0	X	X	X	Low ¹	Low ¹	Off
1	Running	0	X	Low ¹	Low ¹	On ²
1	Running	1	0	Running	Running	On ²
1	Running	1	1	Low ¹	Low ¹	On ²

1. The output state is set by B11[1:0] (Low/Low default)
2. If Bypass mode is selected, the PLL will be off, and outputs will be running.



ADLINK

Part Name :

Type 7 carrier board

Schematic Version : A2.5

A2.5

[illegible]