COM-HPC Server Base

Rev: A2

P/N: 55-77106-000E

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ADLINK CONFIDENTIAL

<Variant Name>

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Title	Cover Page	
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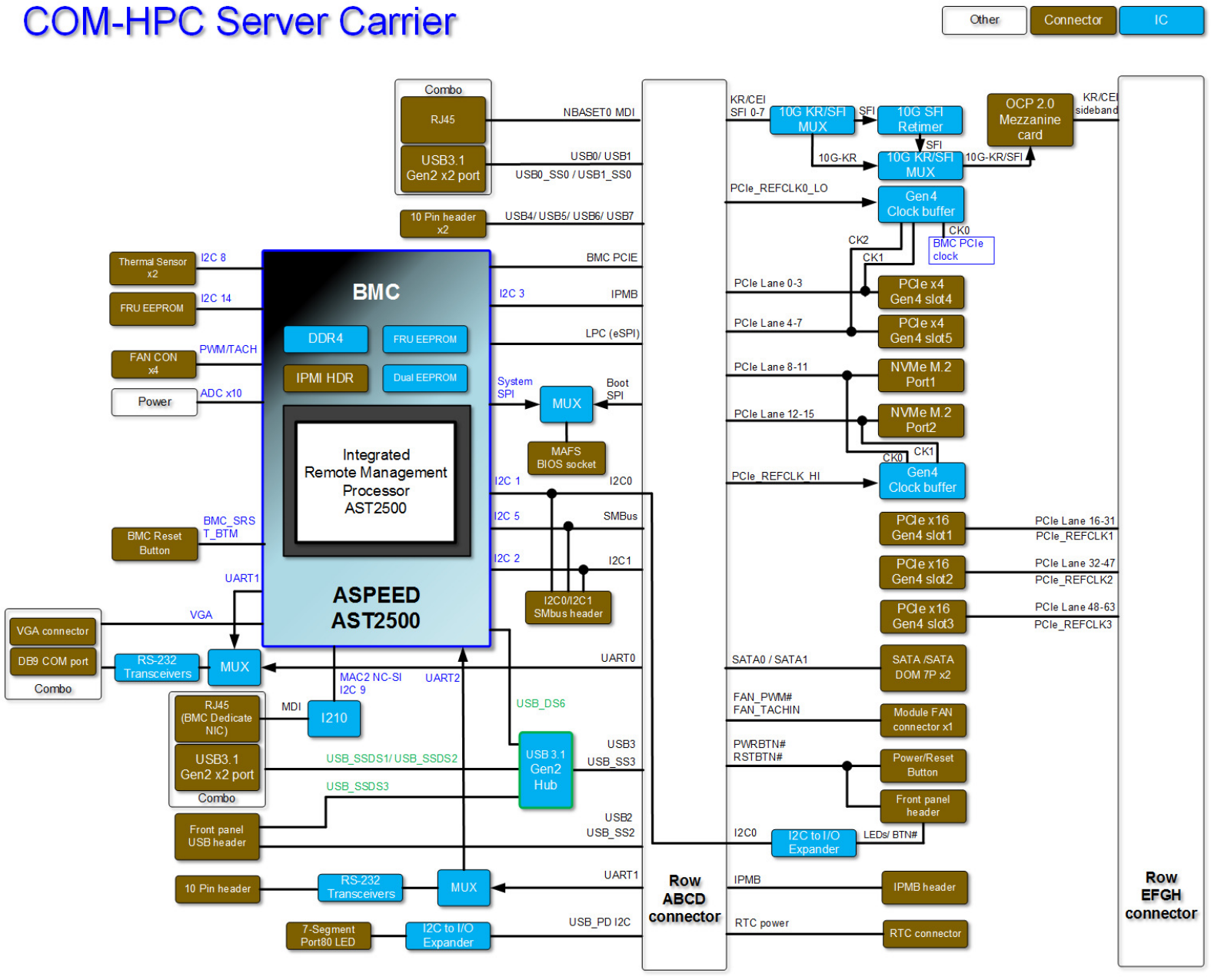
COM-HPC Server Carrier



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Title	Block Diagram	
Size: Custom	Document Number: COM-HPC Server Base	Rev: A1
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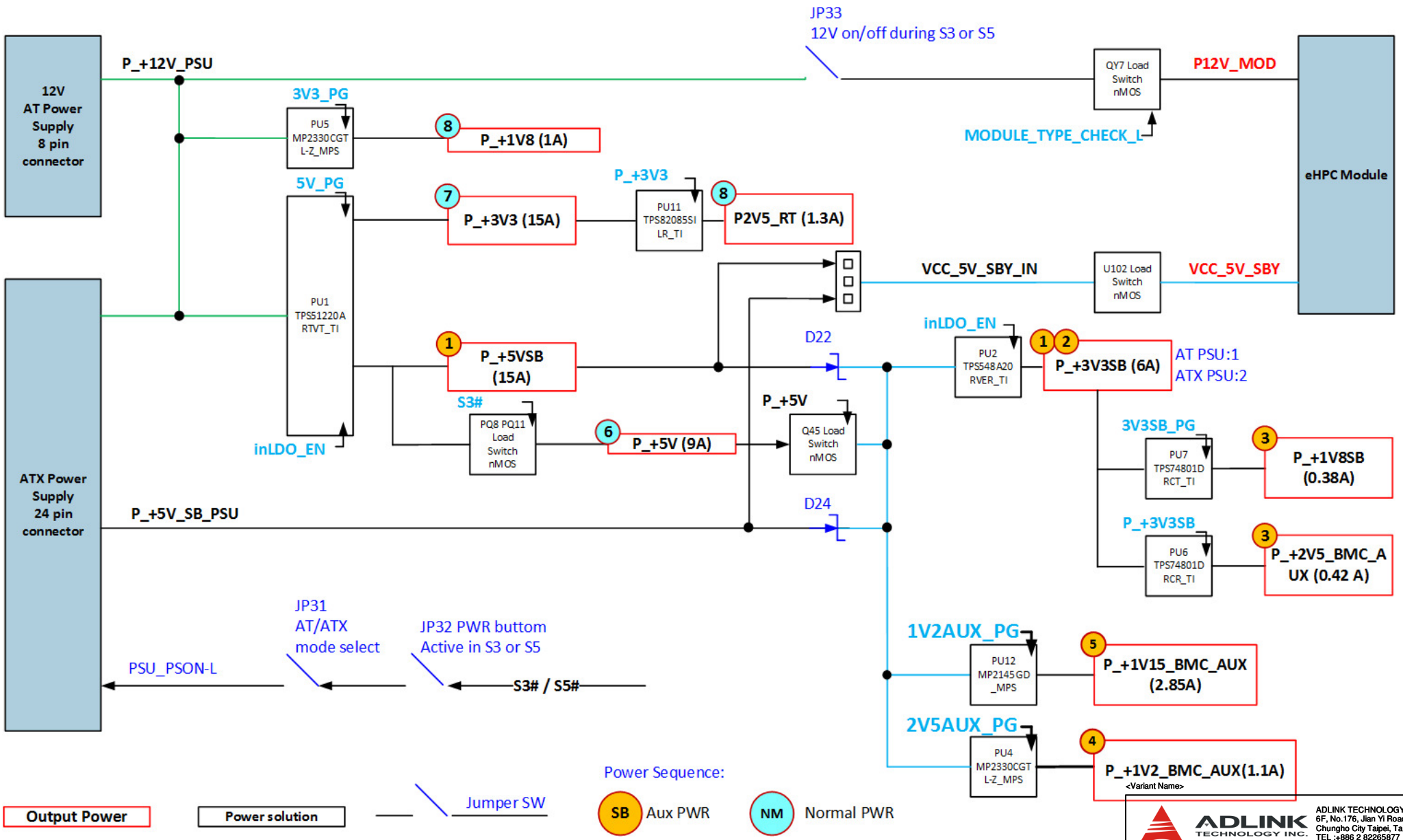
COM-HPC Server Carrier



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Title	Power Delivery	
Size A3	Document Number COM-HPC Server Base	Rev A1
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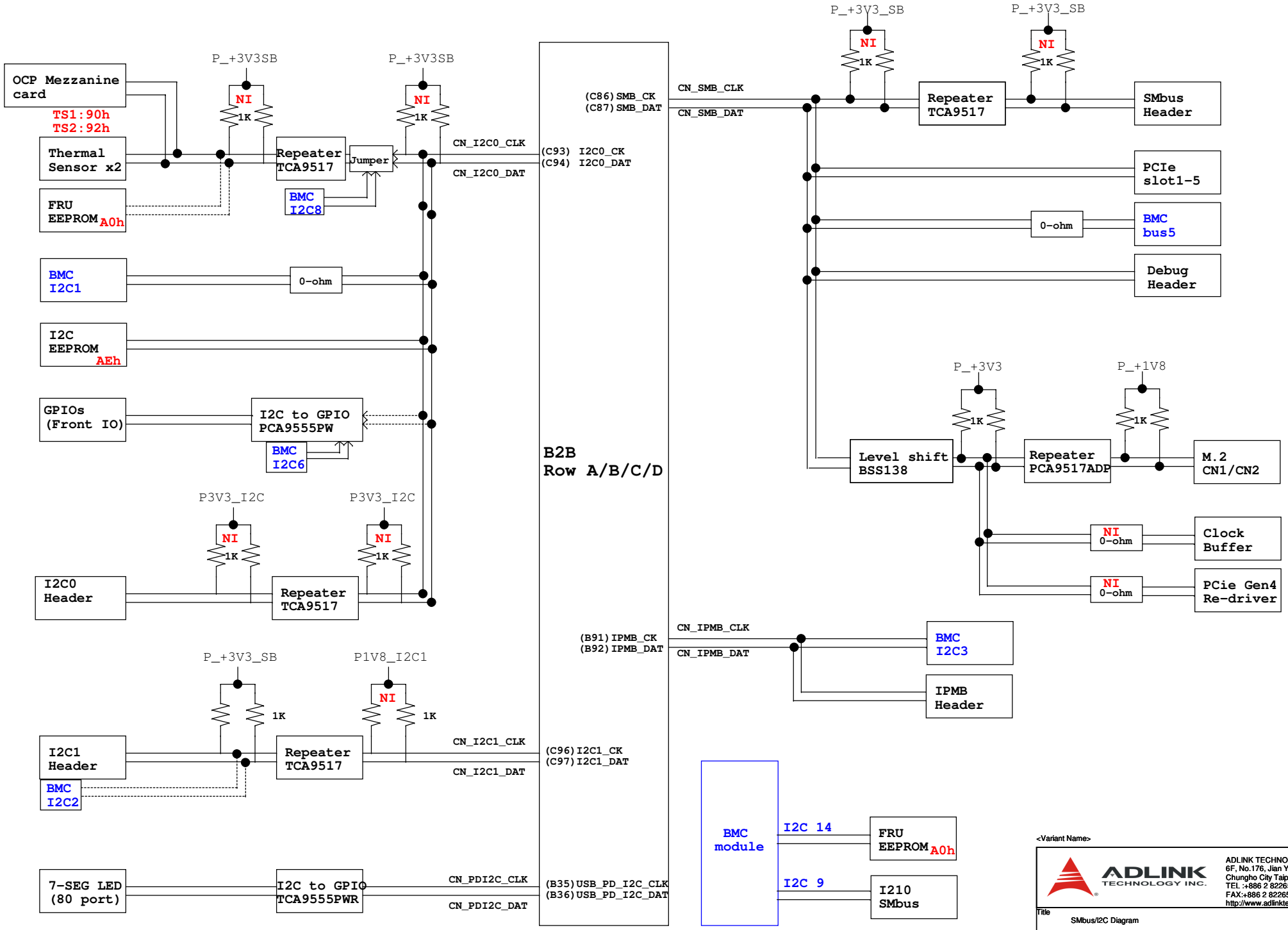

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Title	SMbus/I2C Diagram	
Size A3	Document Number COM-HPC Server Base	Rev A1
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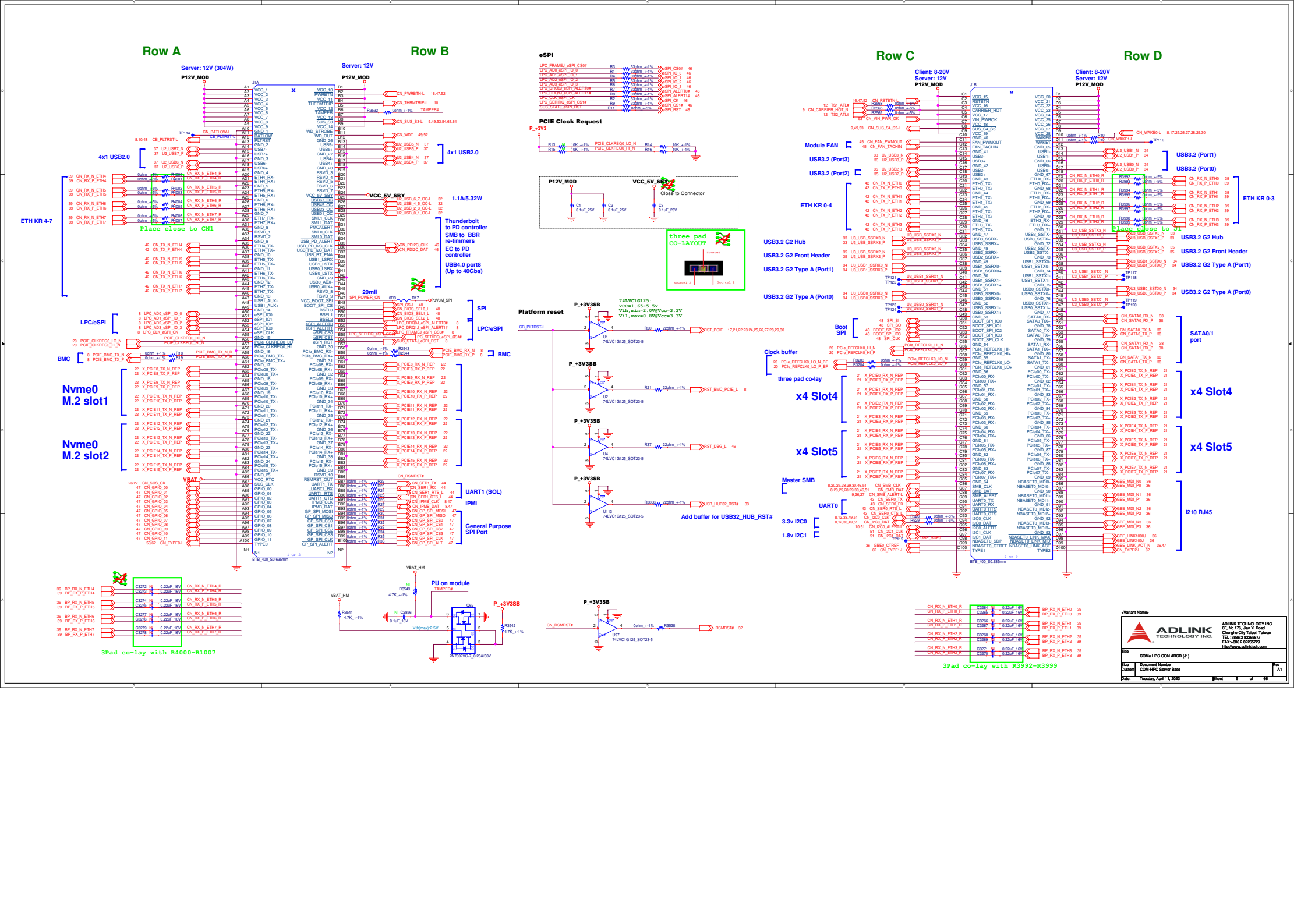
Row A
Row B
Row C
Row D
Server: 12V (304W)
Server: 12V
Client: 8-20V
Server: 12V
P12V_MOD
4x1 USB2.0
ETH KR 4-7
Place close to CN1
LPC/eSPI
BMC
Nvme0
M.2 slot1
Nvme0
M.2 slot2
3Pad co-lay with R4000-R1007
VBAT
PU on module
TAMPER#
1.1A/5.32W
Thunderbolt
to PD controller
SMB to BBR
re-timmers
EC to PD
controller
USB4.0 port8
(Up to 40Gbs)
20mil
SPI
LPC/eSPI
BMC
UART1 (SOL)
IPMI
General Purpose
SPI Port
eSPI
PCIE Clock Request
Platform reset
Add buffer for USB32_HUB_RST#
74LVC1G125:
VCC=1.65~5.5V
Vih,min=2.0V@Vcc=3.3V
Vil,max=0.8V@Vcc=3.3V
Module FAN
USB3.2 (Port3)
USB3.2 (Port2)
ETH KR 0-4
USB3.2 G2 Hub
USB3.2 G2 Front Header
USB3.2 G2 Type A (Port1)
USB3.2 G2 Type A (Port0)
Boot
SPI
Clock buffer
three pad co-lay
x4 Slot4
x4 Slot5
Master SMB
UART0
3.3v I2C0
1.8v I2C1
3Pad co-lay with R3992-R3999
USB3.2 (Port1)
USB3.2 (Port0)
ETH KR 0-3
Place close to J1
USB3.2 G2 Hub
USB3.2 G2 Front Header
USB3.2 G2 Type A (Port1)
USB3.2 G2 Type A (Port0)
SATA0/1
port
x4 Slot4
x4 Slot5
I210 RJ45
ADLINK TECHNOLOGY INC.
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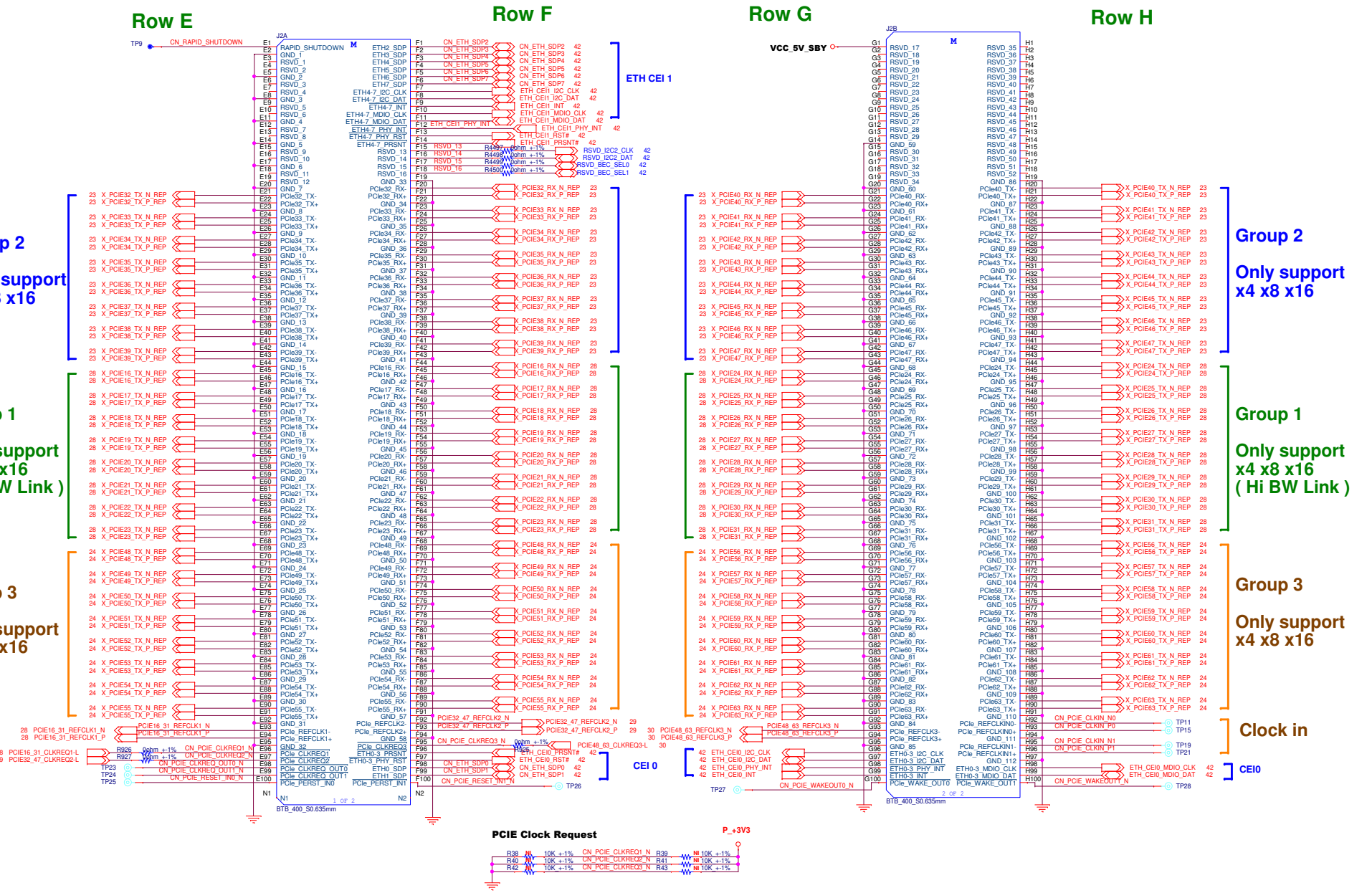
COMe HPC CON ABCD (J1)
COM-HPC Server Base
Tuesday, April 11, 2023



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<Variant Name>		
Title	COMe HPC CON EFGH (J2)	
Size C	Document Number COM-HPC Server Base	Rev A1
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Title

Size	Document Number	Rev
A3	COM-HPC Server Base	A1

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NC or pull low for AST2520

R45 NI X_100K_+-1%

U5A

AST2500/2520 Rev.1.5

PCI-Express

DDR3/DDR4

LPC ESPI

SD/SDIO

I2C

GPIO

1 OF 4

71_AST2500/2520_0

5,10,48 CB_PLTRST-L — R44 NI 0ohm_+-5% — PCIE_BMC_RSTN — L20 PERST

R46 0ohm_+-5%

5 RST_BMC_PCIE_L

20 BMC_REFCLK_100M_P — K21 PEREFCLKP

20 BMC_REFCLK_100M_N — K22 PEREFCLKN

5 PCIE_BMC_TX_P — M21 PERXP

5 PCIE_BMC_TX_N — M22 PERXN

L21 PCIE_BMC_RX_P_C — C4 0.1uF_25V — PCIE_BMC_RX_P 5

L22 PCIE_BMC_RX_N_C — C5 0.1uF_25V — PCIE_BMC_RX_N 5

PETXP

PETXN

PEREXT — K20 PD_P2E_BMC_PEREXT — R47 200ohm_+-1%

P_+3V3SB

U10

13 V_M_BMC_DDR4_DQ0 — W10 MDQ0
13 V_M_BMC_DDR4_DQ1 — Y10 MDQ1
13 V_M_BMC_DDR4_DQ2 — AA10 MDQ2
13 V_M_BMC_DDR4_DQ3 — U9 MDQ3
13 V_M_BMC_DDR4_DQ4 — Y9 MDQ4
13 V_M_BMC_DDR4_DQ5 — W9 MDQ5
13 V_M_BMC_DDR4_DQ6 — V9 MDQ6
13 V_M_BMC_DDR4_DQ7 — AA8 MDQ7
13 V_M_BMC_DDR4_DQ8 — Y8 MDQ8
13 V_M_BMC_DDR4_DQ9 — Y7 MDQ9
13 V_M_BMC_DDR4_DQ10 — W8 MDQ10
13 V_M_BMC_DDR4_DQ11 — AA6 MDQ11
13 V_M_BMC_DDR4_DQ12 — W7 MDQ12
13 V_M_BMC_DDR4_DQ13 — V7 MDQ13
13 V_M_BMC_DDR4_DQ14 — U7 MDQ14
13 V_M_BMC_DDR4_DQ15 — MDQ15

13 V_M_BMC_DDR4_DQS0_DP — AB9 MDQS0
13 V_M_BMC_DDR4_DQS1_DP — AB7 MDQS1
13 V_M_BMC_DDR4_DQS0_DN — AB10 MDQS0
13 V_M_BMC_DDR4_DQS1_DN — AB6 MDQS1

13 V_M_BMC_DDR4_RST_N — AB17 MRESET
13 V_M_BMC_DDR4_ALERT_N — U16 MALERT
P_+1V2_BMC_AUX — R3512 NI 4.7K_+-1%
P0V6_DDR_VREF_AUX — T9 MVREF
C6 0.1uF_25V

R68 240ohm_+-1% — W11 MIOZ

MCK — AB11
MCK — AB12
MCKE — Y11
MODT — V11
MCS — AA12
MRAS — W12
MCAS — AB13
MWE — Y12
MBA0 — U12
MBA1 — Y13
MBA2_MBG0 — W13
MA0 — V13
MA1 — AB14
MA2 — W14
MA3 — U14
MA4 — W15
MA5 — V15
MA6 — AB16
MA7 — AA16
MA8 — W16
MA9 — Y16
MA10 — U13
MA11 — AA14
MA12 — Y14
MA13 — AB15
MA14_MACT — Y15
MA15 — U15
MDM0 — U8
MDM1 — AB8

V_M_BMC_DDR4_CLK_DP 13
V_M_BMC_DDR4_CLK_DN 13
V_M_BMC_DDR4_CKE 13
V_M_BMC_DDR4_ODT 13
V_M_BMC_DDR4_CS_N 13
V_M_BMC_DDR4_MA16 13
V_M_BMC_DDR4_MA15 13
V_M_BMC_DDR4_MA14 13
V_M_BMC_DDR4_BA0 13
V_M_BMC_DDR4_BA1 13
V_M_BMC_DDR4_BG0 13
V_M_BMC_DDR4_MA0 13
V_M_BMC_DDR4_MA1 13
V_M_BMC_DDR4_MA2 13
V_M_BMC_DDR4_MA3 13
V_M_BMC_DDR4_MA4 13
V_M_BMC_DDR4_MA5 13
V_M_BMC_DDR4_MA6 13
V_M_BMC_DDR4_MA7 13
V_M_BMC_DDR4_MA8 13
V_M_BMC_DDR4_MA9 13
V_M_BMC_DDR4_MA10 13
V_M_BMC_DDR4_MA11 13
V_M_BMC_DDR4_MA12 13
V_M_BMC_DDR4_MA13 13
V_M_BMC_DDR4_ACT_N 13
V_M_BMC_DDR4_DM0 13
V_M_BMC_DDR4_DM1 13

BMC_SCL1 — R48 NI X_4.7K_+-1%
BMC_SDA1 — R49 NI X_4.7K_+-1%
BMC_SCL2 — R50 NI X_4.7K_+-1%
BMC_SDA2 — R51 NI X_4.7K_+-1%
BMC_SCL3 — R52 NI 4.7K_+-1%
BMC_SDA3 — R53 NI 4.7K_+-1%
BMC_SCL5 — R56 NI X_4.7K_+-1%
BMC_SDA5 — R57 NI X_4.7K_+-1%
BMC_SCL6 — R58 X_4.7K_+-1%
BMC_SDA6 — R59 X_4.7K_+-1%
BMC_SCL7 — R60 X_4.7K_+-1%
BMC_SDA7 — R61 X_4.7K_+-1%
BMC_SCL8 — R62 NI X_4.7K_+-1%
BMC_SDA8 — R63 NI X_4.7K_+-1%
BMC_SCL9 — R64 4.7K_+-1%
BMC_SDA9 — R65 4.7K_+-1%

5 LPC_CLK_eSPI_CK — R70 0ohm_+-5% — BMC_LCK
5 LPC_FRAMEJ_eSPI_CS0# — R72 0ohm_+-5% — C22 GPIOAC4_ESPICK_LCLK
5 LPC_SERIRQ_eSPI_CS1# — R74 NI 0ohm_+-5% — BMC_LFRAME — F21 GPIOAC5_ESPICS_LFRAME
5 LPC_DRQ0J_eSPI_ALERT0# — R76 33ohm_+-1% — BMC_LSIRQ — F22 GPIOAC6_ESPIALT_LSIRQ
5 LPC_DRQ1J_eSPI_ALERT1# — R78 NI 33ohm_+-1% — G22 GPIOAC7_ESPIRST_LPCRST
5 SUS_STATJ_eSPI_RST — R80 0ohm_+-5% — BMC_LPCRST

R70,R72-80 need to change to33ohm with eSPI interface

J20 GPIOB4_USBCKI — H21 GPIOB5_LPCPD_LPCSMI — H22 GPIOB6_LPCPME — H20 GPIOB7

P_+3V3SB — R81 10K_+-1% — LPC_PME_N

G21 BMC_LAD0 — R73 33ohm_+-1% — LPC_AD0_eSPI_IO_0 5
G20 BMC_LAD1 — R75 33ohm_+-1% — LPC_AD1_eSPI_IO_1 5
D22 BMC_LAD2 — R77 33ohm_+-1% — LPC_AD2_eSPI_IO_2 5
E22 BMC_LAD3 — R79 33ohm_+-1% — LPC_AD3_eSPI_IO_3 5

GPIOAC0_ESPID0_LAD0
GPIOAC1_ESPID1_LAD1
GPIOAC2_ESPID2_LAD2
GPIOAC3_ESPID3_LAD3

GPIOB0 — K19
GPIOB1 — L19
GPIOB2 — L18
GPIOB3 — K18

C12 GPIOC0_SD1CLK_SCL10
A12 GPIOC1_SD1CMD_SDA10
B12 GPIOC2_SD1DAT0_SCL11
D9 GPIOC3_SD1DAT1_SDA11
D10 GPIOC4_SD1DAT2_SCL12
E12 GPIOC5_SD1DAT3_SDA12
C11 GPIOC6_SD1CD_SCL13
B11 GPIOC7_SD1WP_SDA13

F19 GPIOD0_SD2CLK
E21 GPIOD1_SD2CMD
F20 GPIOD2_SD2DAT0
D20 GPIOD3_SD2DAT1
D21 GPIOD4_SD2DAT2
E20 GPIOD5_SD2DAT3
G18 GPIOD6_SD2CD
C21 GPIOD7_SD2WP

GPIOY4_SCL1
GPIOY5_SDA1
GPIOY6_SCL2
GPIOY7_SDA2
GPIOQ0_SCL3
GPIOQ1_SDA3
GPIOQ2_SCL4
GPIOQ3_SDA4

GPIOK0_SCL5
GPIOK1_SDA5
GPIOK2_SCL6
GPIOK3_SDA6
GPIOK4_SCL7
GPIOK5_SDA7
GPIOK6_SCL8
GPIOK7_SDA8
GPIOA4_TIMER5_SCL9
GPIOA5_TIMER6_SDA9

M18 BMC_SCL1 — R82 0ohm_+-5% — CN_I2C0_CLK 5,12,33,49,51
M19 BMC_SDA1 — R83 0ohm_+-5% — CN_I2C0_DAT 5,12,33,49,51 — Module I2C0
M20 BMC_SCL2 — R84 0ohm_+-5% — LV_I2C1_CLK 51
P20 BMC_SDA2 — R85 0ohm_+-5% — LV_I2C1_DAT 51 — Module I2C1 (reserved)
A11 BMC_SCL3 — R86 0ohm_+-5% — CN_IPMB_CLK 5,47
A10 BMC_SDA3 — R87 0ohm_+-5% — CN_IPMB_DAT 5,47 — IPMB

A9 — MEZZ card
B9

L3 BMC_SCL5 — R90 0ohm_+-5% — CN_SMB_CLK 5,20,25,28,29,30,46,51 — Module SMbus
L4 BMC_SDA5 — R91 0ohm_+-5% — CN_SMB_DAT 5,20,25,28,29,30,46,51
L1 BMC_SCL6 — R92 0ohm_+-5% — BMC_SCL6_GPIO 49
N2 BMC_SDA6 — R93 0ohm_+-5% — BMC_SDA6_GPIO 49
N1 BMC_SCL7 — R94 0ohm_+-5% — BMC_FRU_SCL7 12
P1 BMC_SDA7 — R95 0ohm_+-5% — BMC_FRU_SDA7 12 — FRU EEPROM
P2 BMC_SCL8 — R96 0ohm_+-5% — SMB_SENSOR_STBY_LVC3_SCL 12
R1 BMC_SDA8 — R97 0ohm_+-5% — SMB_SENSOR_STBY_LVC3_SDA 12 — Thermal sensor
C14 BMC_SCL9 — R98 0ohm_+-5% — LAN_CLK 17
A13 BMC_SDA9 — R99 0ohm_+-5% — LAN_DAT 17 — LAN Chip

TP209 — GPIOA0 — B14 GPIOA0_MAC1LINK
TP210 — GPIOA1 — D14 GPIOA1_MAC2LINK
TP211 — GPIOA2 — D13 GPIOA2_TIMER3_SPI1CS1
TP212 — GPIOA3 — E13 GPIOA3_TIMER4

GPIOQ4_SCL14
GPIOQ5_SDA14
GPIOQ6_OSCCLK
GPIOQ7_PEWAKE

N21
N22
B10
N20 — R3516 NI 0ohm_+-5% — CN_WAKE0-L 5,17,25,26,27,28,29,30
R3515 NI X_4.7K_+-1% — P_+3V3SB

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Block: BMC (PCIE_DDR_I2C_SD_LPC)

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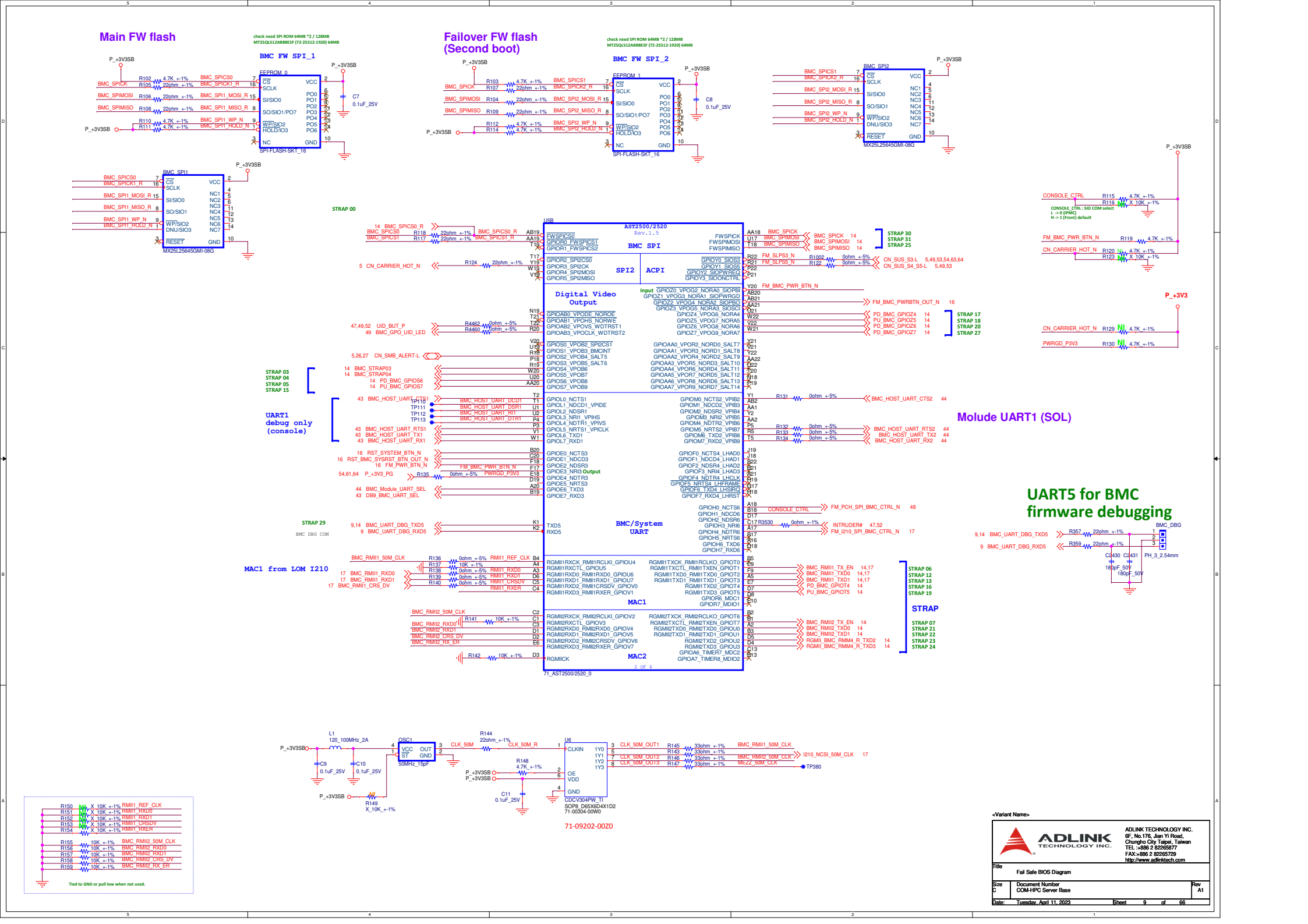

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<Variant Name>

Title	Fail Safe BIOS Diagram	
Size C	Document Number COM-HPC Server Base	Rev A1
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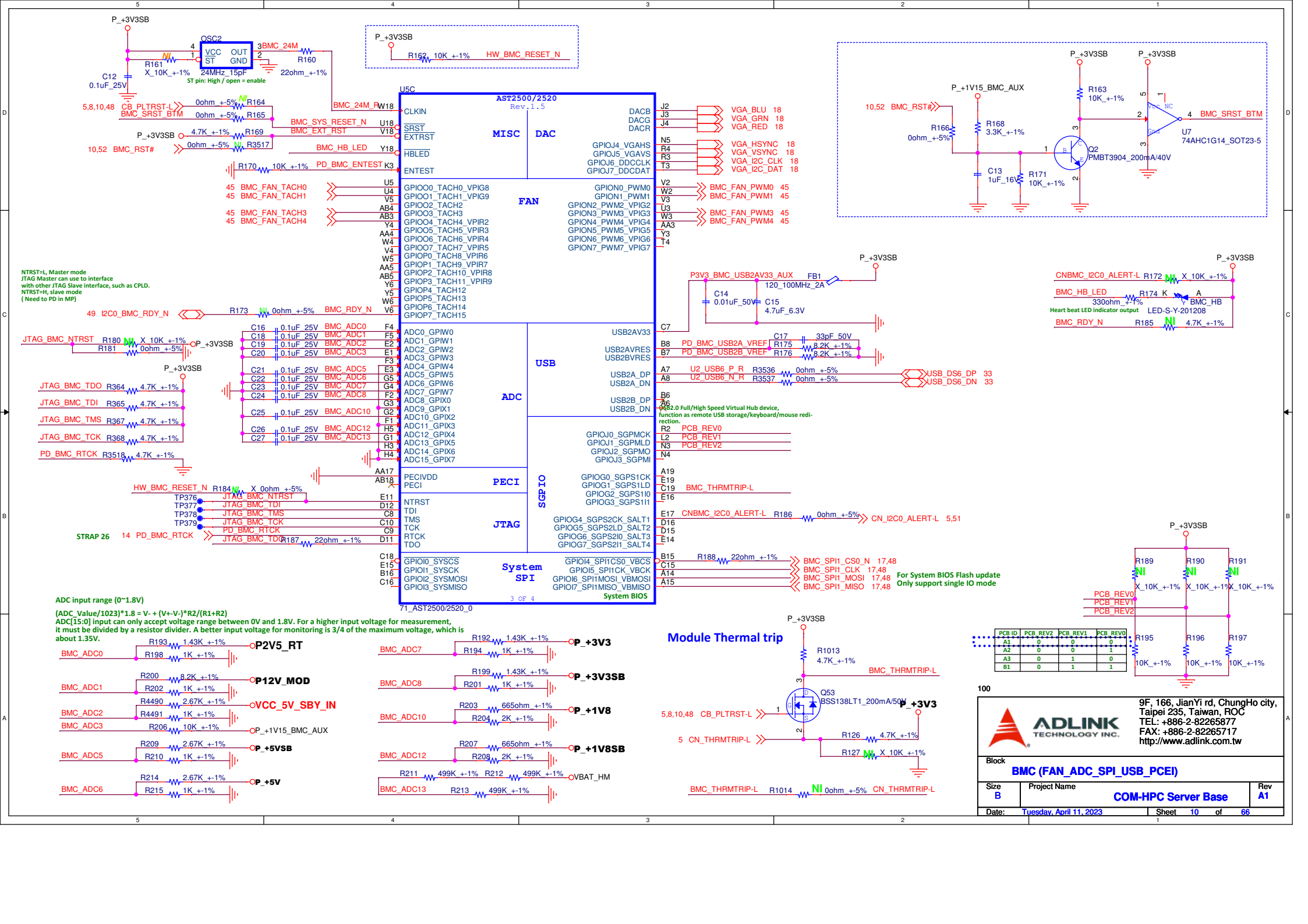
U5C
AST2500/2520
Rev.1.5
MISC
DAC
FAN
ADC
USB
PECI
JTAG
SGPIO
System SPI
3 OF 4
71_AST2500/2520_0
OSC2
24MHz_15pF
ST pin: High / open = enable
NTRST=L, Master mode
JTAG Master can use to interface with other JTAG Slave interface, such as CPLD.
NTRST=H, slave mode
(Need to PD in MP)
ADC input range (0~1.8V)
(ADC_Value/1023)*1.8 = V- + (V+-V-)*R2/(R1+R2)
ADC[15:0] input can only accept voltage range between 0V and 1.8V. For a higher input voltage for measurement, it must be divided by a resistor divider. A better input voltage for monitoring is 3/4 of the maximum voltage, which is about 1.35V.
P2V5_RT
P12V_MOD
VCC_5V_SBY_IN
P_+1V15_BMC_AUX
P_+5VSB
P_+5V
P_+3V3
P_+3V3SB
P_+1V8
P_+1V8SB
VBAT_HM
Module Thermal trip
Q53
BSS138LT1_200mA/50V
Q2
PMBT3904_200mA/40V
U7
74AHC1G14_SOT23-5
USB2.0 Full/High Speed Virtual Hub device, function as remote USB storage/keyboard/mouse redirection.
For System BIOS Flash update
Only support single IO mode
System BIOS
STRAP 26
Heart beat LED indicator output
LED-S-Y-201208
ADLINK TECHNOLOGY INC.
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Block
BMC (FAN_ADC_SPI_USB_PCEI)
Size
B
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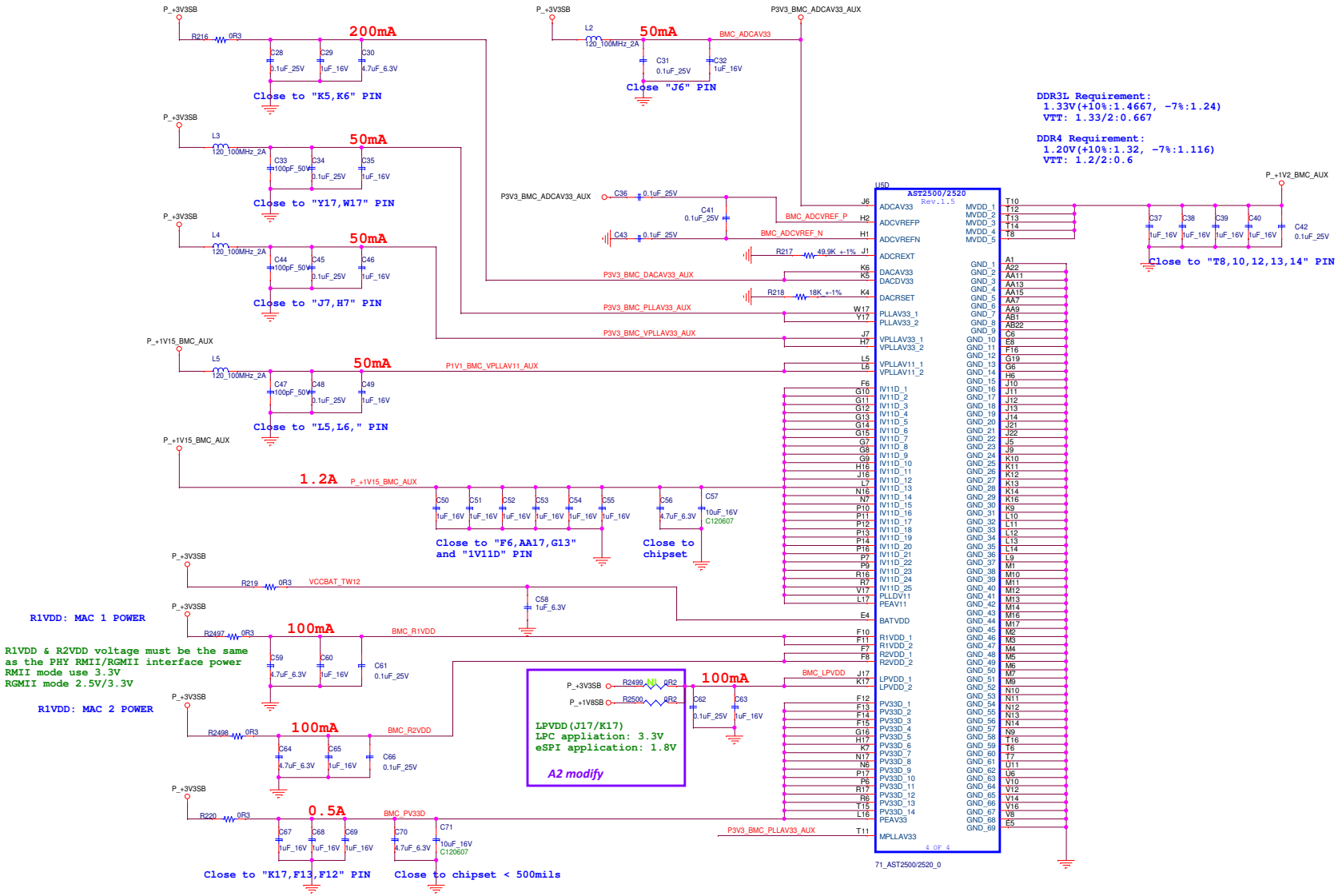

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Block: BMC (PWR)		
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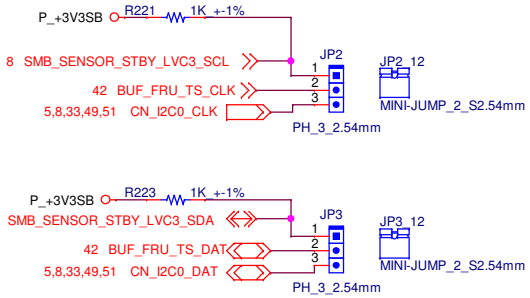
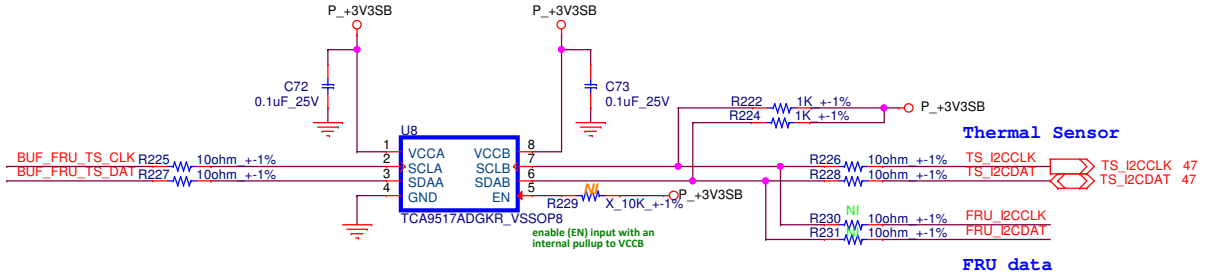
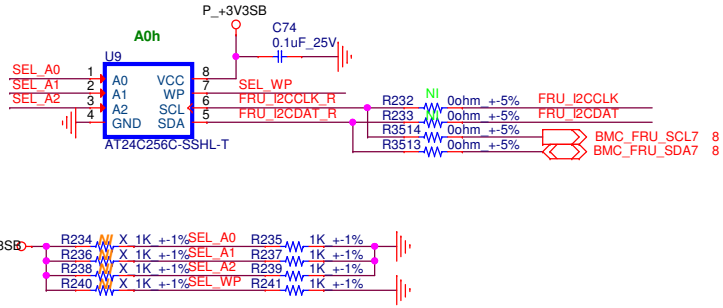
BMC I2C8 / Module I2C0

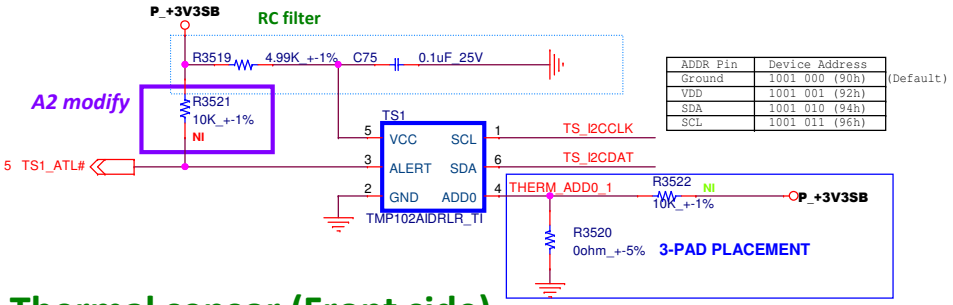




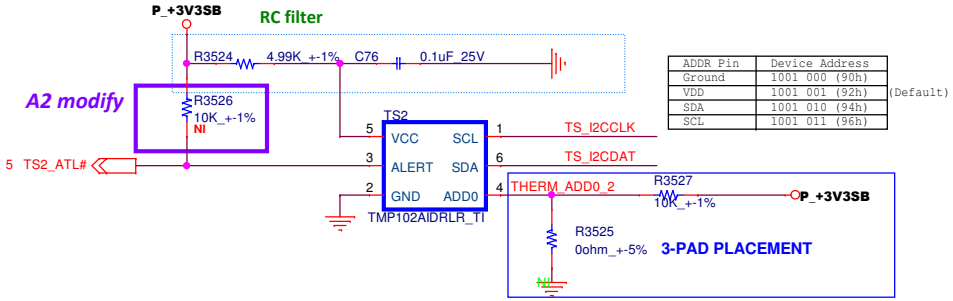
FRU EEPROM



Thermal sensor (Rear side)



Thermal sensor (Front side)



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Block	BMC JTAG HEADER	
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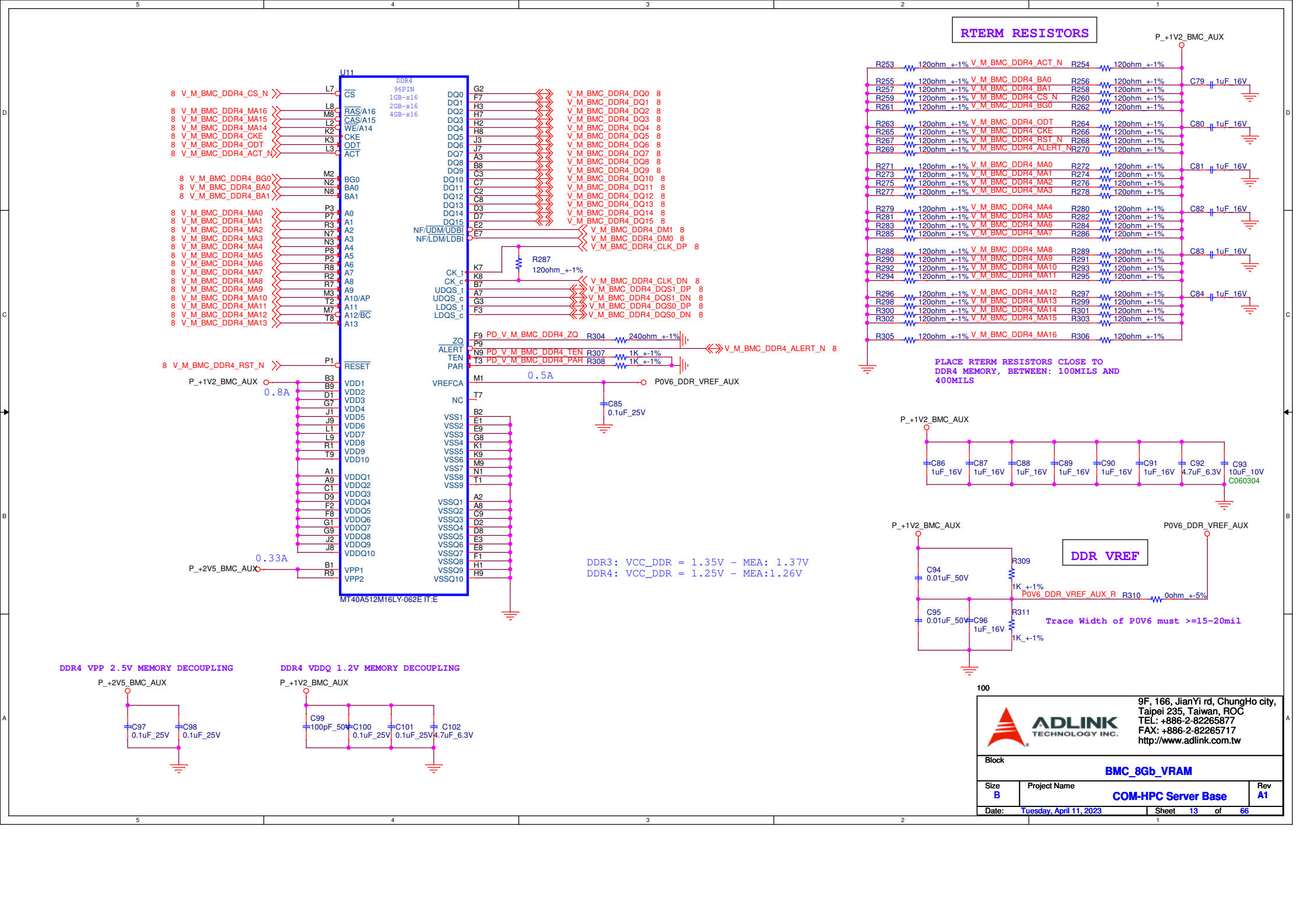
RTERM RESISTORS
U11
DDR4
96PIN
1GB-x16
2GB-x16
4GB-x16
MT40A512M16LY-062E IT:E
P_+1V2_BMC_AUX
P_+2V5_BMC_AUX
P0V6_DDR_VREF_AUX
PLACE RTERM RESISTORS CLOSE TO DDR4 MEMORY, BETWEEN: 100MILS AND 400MILS
DDR VREF
Trace Width of P0V6 must >=15-20mil
DDR3: VCC_DDR = 1.35V - MEA: 1.37V
DDR4: VCC_DDR = 1.25V - MEA:1.26V
DDR4 VPP 2.5V MEMORY DECOUPLING
DDR4 VDDQ 1.2V MEMORY DECOUPLING
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Block
BMC_8Gb_VRAM
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FOR ALMOST ALL STRAPS, NO PULL-UP MEANS '0' AND PULL-UP MEANS '1'.

FOR RGMII'S STRAPS (6, 7, 12, 13, 16, 19, 21, 22, 23, 24), PULL-UP MEANS '1' AND PULL-DOWN MEANS '0'.

STRAP NUM	BALL NUM	BALL NAME	DESCRIPTION
31	U17	FWSPIMOSI	ENABLE SPI FLASH STRAP AUTO FETCH MODE 0: DISABLE 1: ENABLE (DFLT)
30	AA18	FWSPICK	ENABLE GPIO STRAP MODE 0: DISABLE 1: ENABLE (DFLT)
29	K1	TXD5	SELECT UART DEBUG PORT (IT CAN SUPPORT FIRMWARE UPDATE CAPABILITY) 0: SELECT UART1 AS BMC CONSOLE PORT 1: SELECT UART5 AS BMC CONSOLE PORT (DFLT)
27	W21	GPIOZ7	ENABLE FAST RESET MODE FOR ARM ICE DEBUGGER 0: LONG RESET MODE, NORMAL OPERATION (DFLT)1: FAST RESET MODE, FOR ICE DEBUGGER CONNECTION
26	C9	RTCK	ENABLE ESPI FLASH MODE (BIT VALID ONLY WHEN ESPI MODE IS ENABLE) 0: ESPI RESPOND WITH NO FLASH ATTACHED (DFLT)1: ESPI RESPOND WITH FLASH ATTACHED
25	T18	FWSPIMISO	ENABLE ESPI MODE 0: LPC MODE 1: ESPI MODE (DFLT)
24	D4	RGMII2TXD3	SELECT DDR4 SDRAM 0: DDR3 SDRAM 1: DDR4 SDRAM (DFLT)
23	D5	RGMII2TXD2	SELECT 25MHZ REFERENCE CLOCK INPUT MODE 0: CLKIN IS 24MHZ AND USBCKI NOT USED 1: CLKIN IS 25MHZ AND USBCKI = 24/48MHZ (DFLT)
22	B3	RGMII2TXD1	ENABLE GPIOE PASS-THROUGH MODE 0: DISABLE 1: ENABLE PASS-THRU AT POWER ON (DFLT)
21	A2	RGMII2TXD0	ENABLE GPIOD PASS-THROUGH MODE 0: DISABLE 1: ENABLE PASS-THRU AT POWER ON (DFLT)
20	V22	GPIOZ6	DISABLE LPC TO DECODE SUPER-IO 0X2E/0X4E ADDRESS 0: ENABLE ADDRESS DECODING (DFLT) 1: DISABLE ADDRESS DECODING
19	D7	RGMII1TXD3	ENABLE ACPI FUNCTION 0: DISABLE ACPI 1: ENABLE ACPI (DFLT)
18	W22	GPIOZ5	SELECT USBCKI INPUT FREQUENCY 0: 24MHZ 1: 48MHZ (DFLT)
17	U21	GPIOZ4	ENABLE BMC 2ND BOOT WATCHDOG TIMER 0: DISABLE (DFLT) 1: ENABLE TIMER START COUNTING AT POWER UP
16	E7	RGMII1TXD2	SUPER-IO CONFIGURATION ADDRESS SELECTION 0: DECODE 0X2E (DFLT) 1: DECODE 0X4E
15	AA20	GPIOS7	VGA CLASS CODE SELECTION 0: SELECT THE CLASS CODE FOR VIDEO DEVICE 1: SELECT THE CLASS CODE FOR VGA DEVICE (DFLT)
13	A2	RGMII1TXD1	SPI MODE SELECTION [13:12] (RELATED TO GPIOI[7:4]) 00: DISABLE SPI INTERFACE (DFLT) 01: ENABLE SPI MASTER 10: ENABLE SPI MASTER AND SPI SLAVE TO AHB BRIDGE 11: ENABLE SPI PASS-THROUGH
12	F9	RGMII1TXD0	
07	B1	RGMII2TXCTL	DEFINE MAC2 INTERFACE 0: RMII/NCSI 1: RGMII (DFLT)
06	E9	RGMII1TXCTL	DFINE MAC1 INTERFACE 0: RMII/NCSI (DFLT) 1: RGMII
05	U20	GPIOS6	ENABLE DEICATED VGA BIOS ROM 0: NO VGA BIOS ROM, VGA BIOS IS MERGED IN THE SYSTEM BIOS (DFLT)1: ENABLE DEDICATED VGA BIOS ROM
04	W20	GPIOS5	RESERVED (0)
03	R19	GPIOS4	VGA MEMORY SIZE [3:2] (ALONG WITH SOFT STRAP 2) 00: SELECT 8MB VGA MEMORY 01: SELECT 16MB VGA MEMORY (DFLT) 10: SELECT 32MB VGA MEMORY 11: SELECT 64MB VGA MEMORY
00	AB19	FWSPICS0#	DISABLE CPU BOOT 0: ENABLE BOOT (DFLT) 1: DISABLE CPU OPERATION, WHEN NO FIRMWARE EXIST

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Block
eSPI Buffer

Size	Project Name	Rev
Custom	**COM-HPC Server Base**	**A1**

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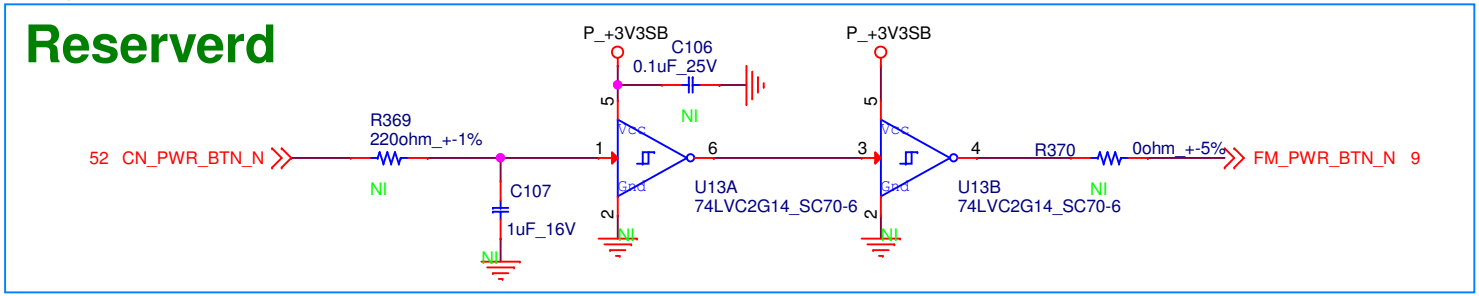
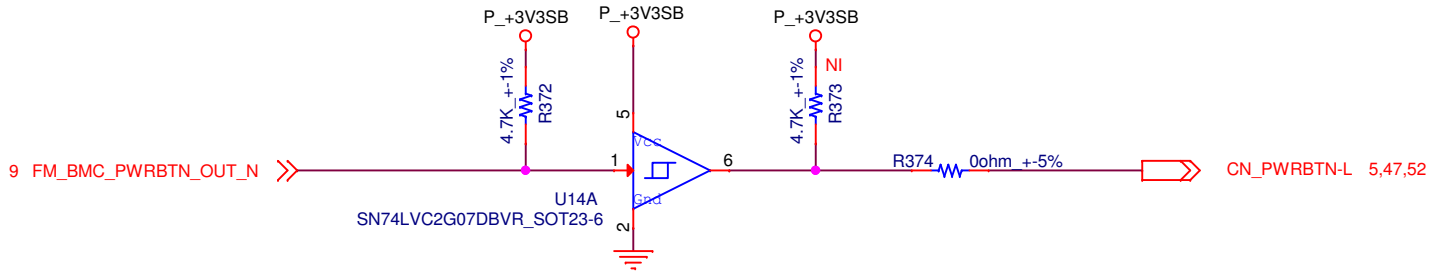
BMC FW power button

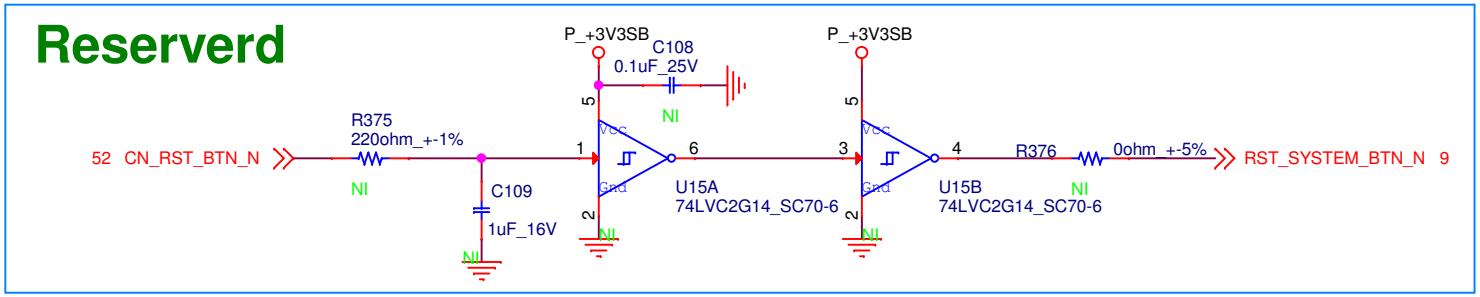
Reserverd

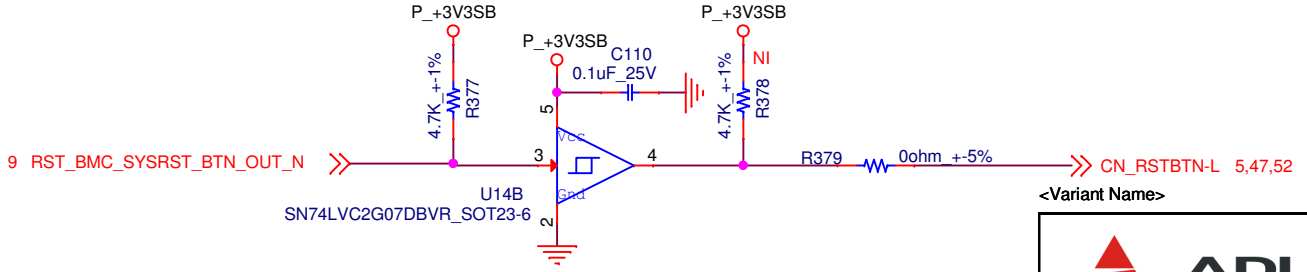




BMC FW power Reset

Reserverd





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Title	BMC FW Buttons	
Size A4	Document Number COM-HPC Server Base	Rev A1
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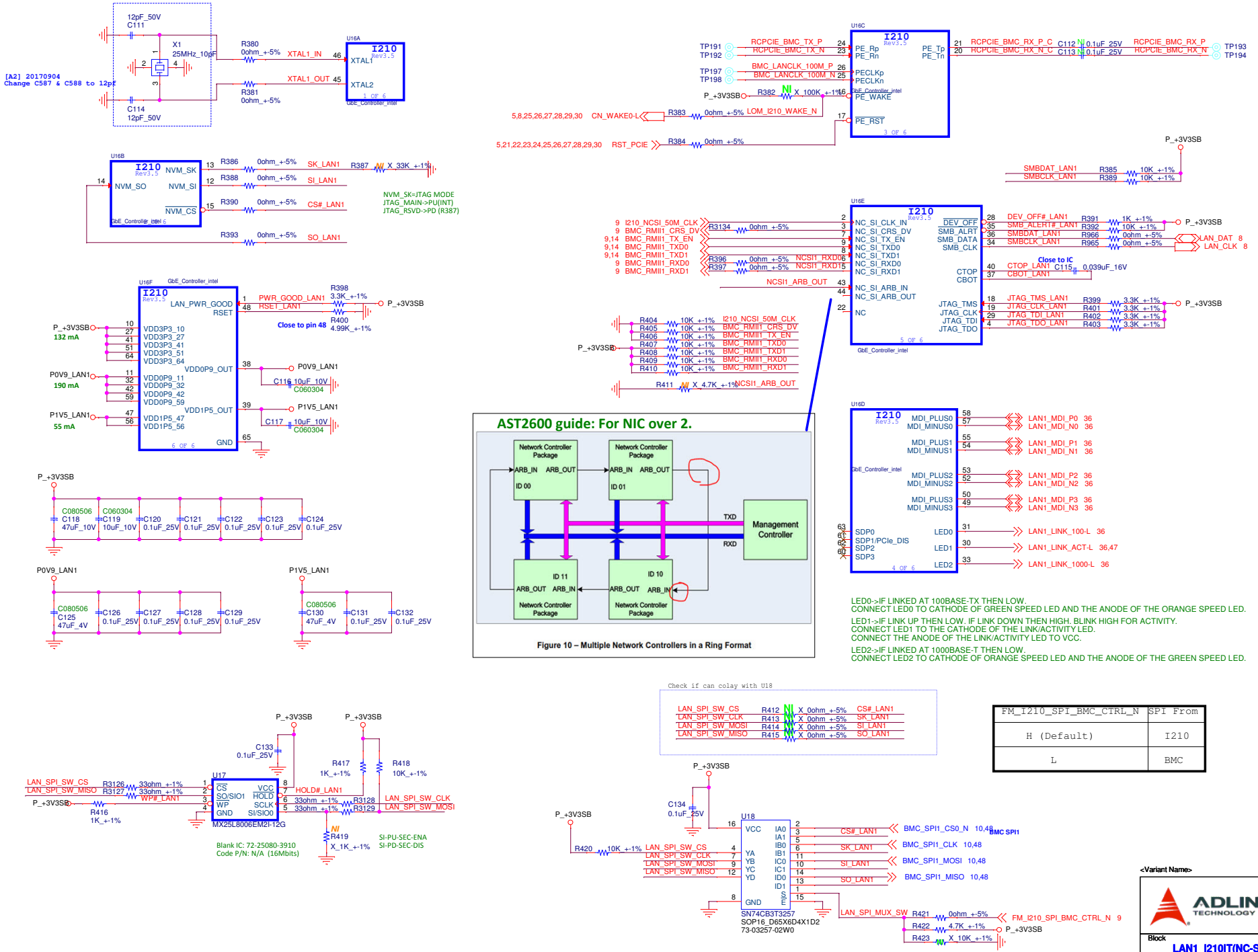

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Size	Custom
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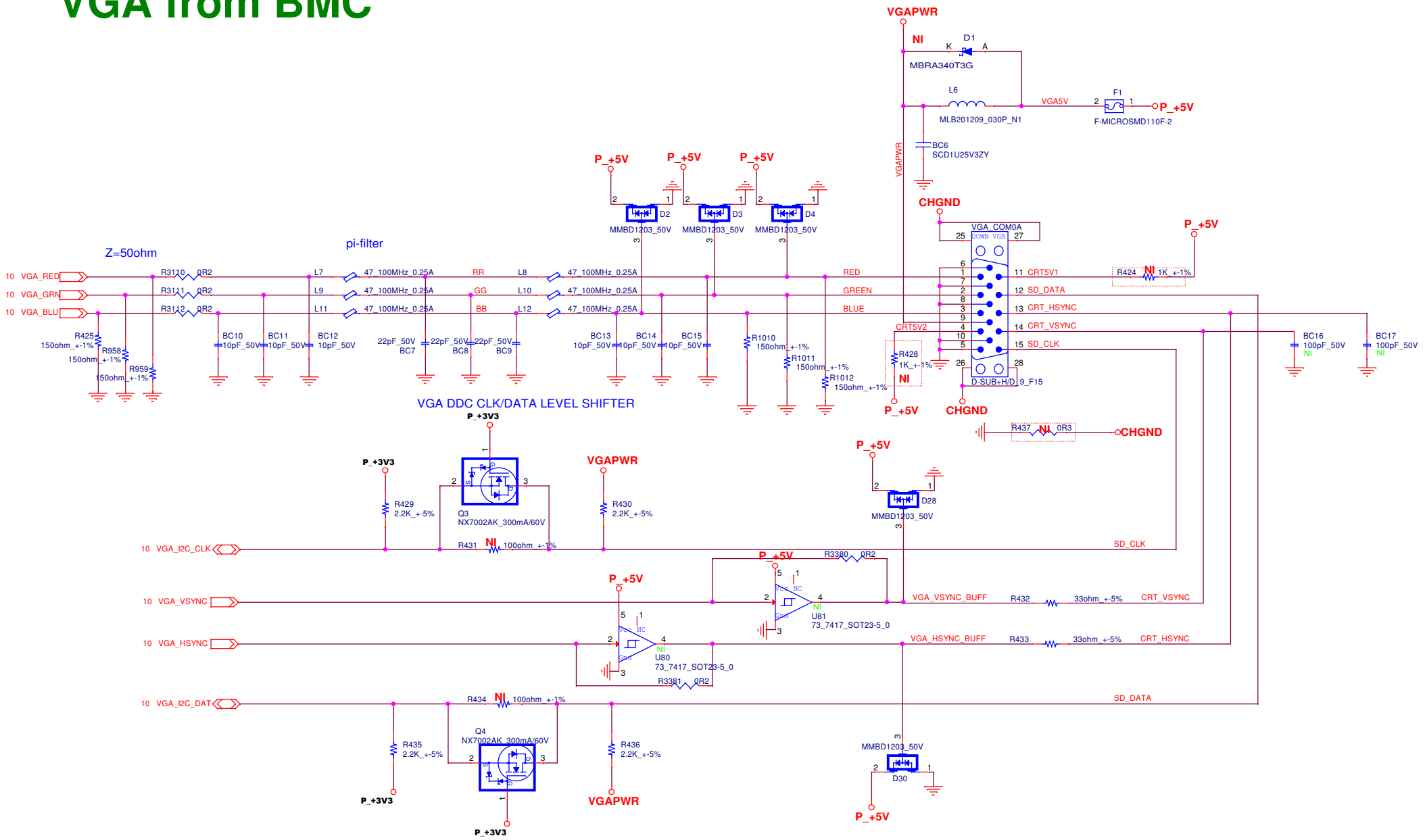
VGA from BMC



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Title	VGA from BMC	
Size A3	Document Number COM-HPC Server Base	Rev A1
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Title

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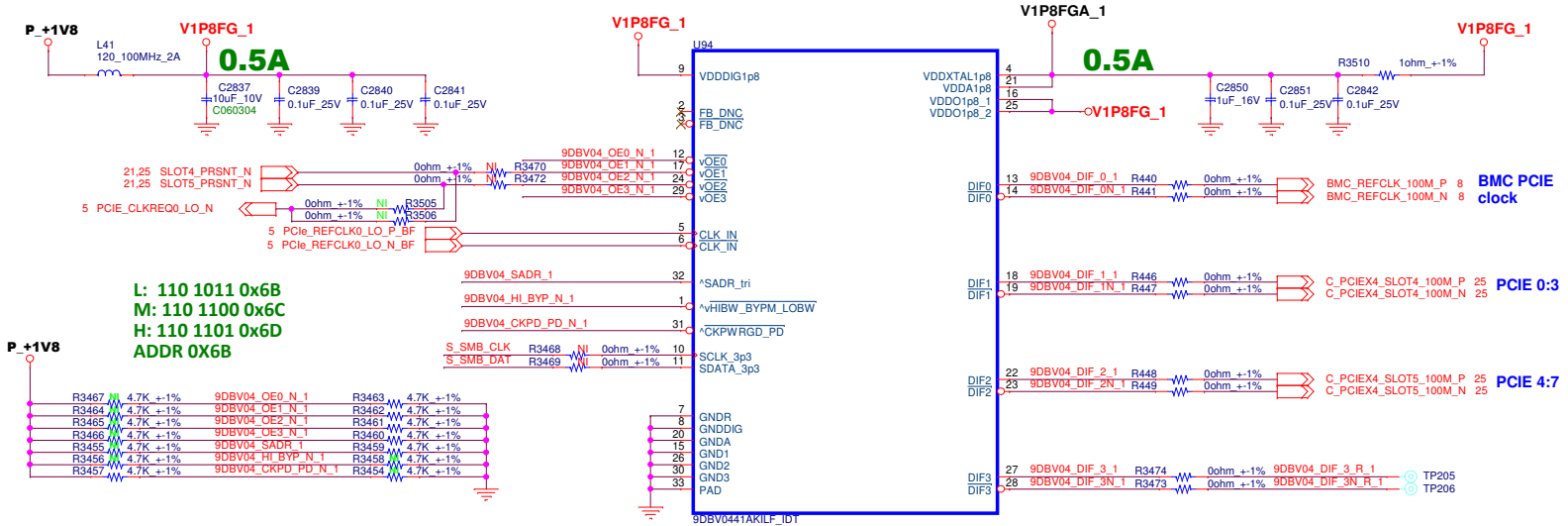
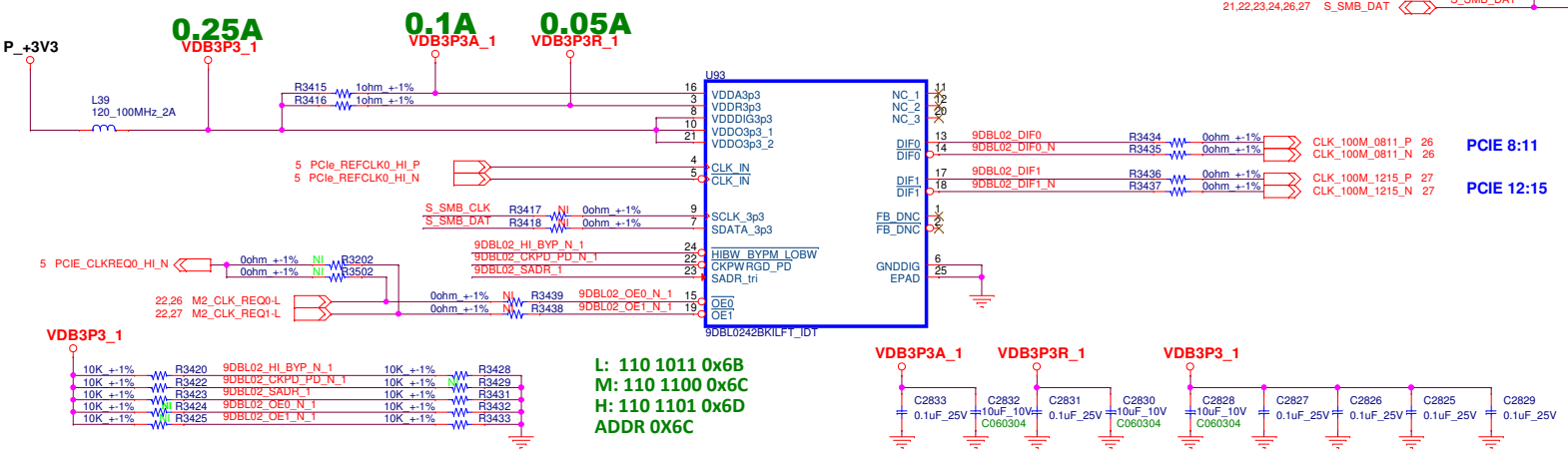
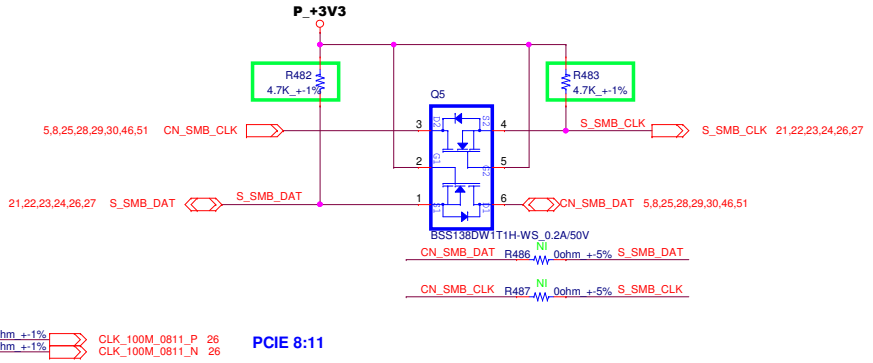
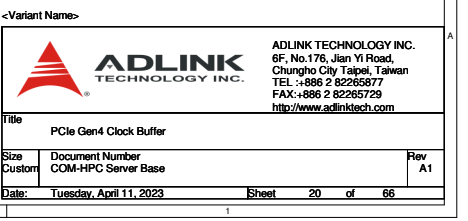
PCIE clock Buffer (100 OHM)



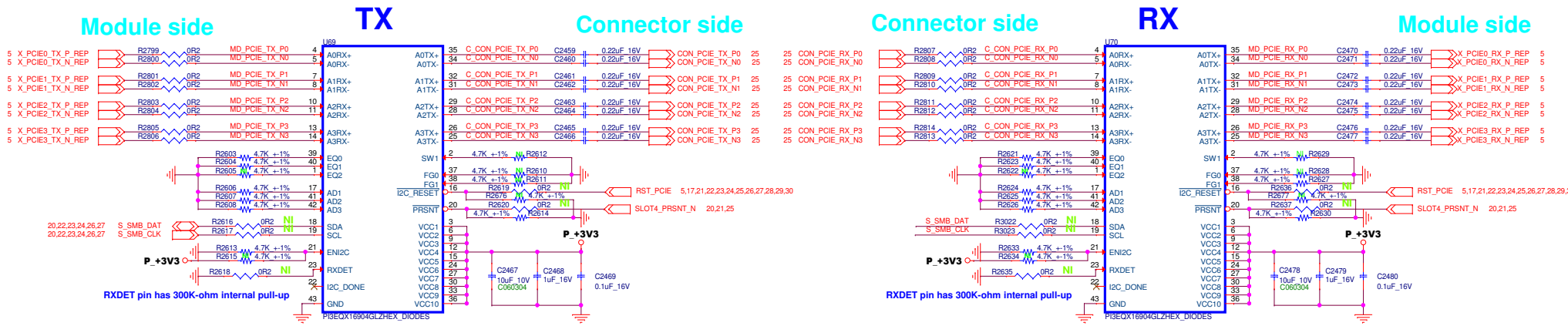
PCIE clock Buffer (100 OHM)







PCIe x4 Slot4 (PCIe 0-3) re-driver



PCIe x4 Slot7 (PCIe 4-7) re-driver

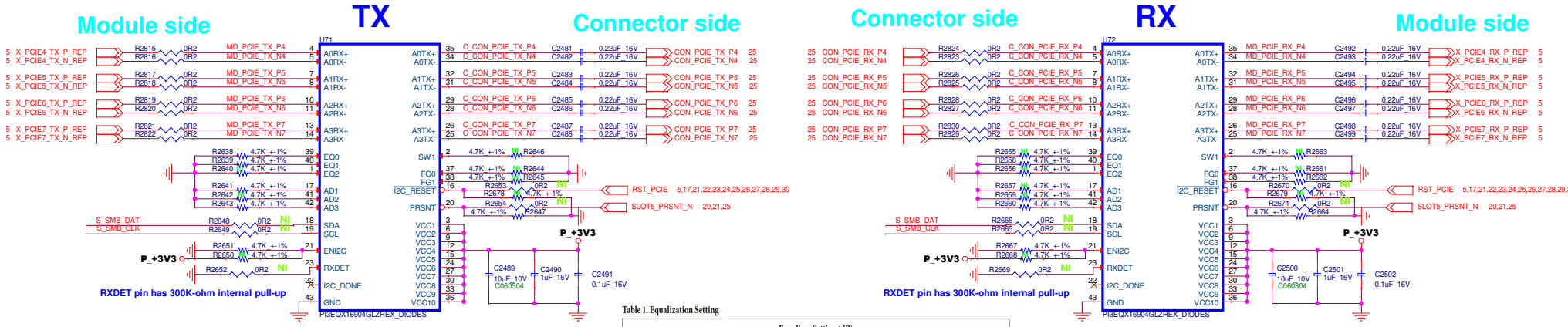


Table 3. Swing Setting

Output Swing Setting		
SW1	SW0	mVp-p
0	0	800
0	1	1000
1	0	1100
1	1	1200

Note: SW0 is from I2C, SW1 is from pin or I2C.

Table 2. Flat Gain Setting

Flat Gain Setting		
FG1	FG0	dB
0	0	-3.5
0	1	-2
1	0	-0.5
1	1	1

Table 1. Equalization Setting

Equalizer Setting (dB)						
EQ2	EQ1	EQ0	@1.25GHz	@2.5GHz	@4GHz	@8GHz
0	0	0	0.2	1.0	2.3	5.6
0	0	1	0.2	1.1	2.6	6.2
0	1	0	1.8	2.7	3.9	7.0
0	1	1	2.1	3.3	4.8	8.5
1	0	0	3.0	4.2	5.8	9.4
1	0	1	3.2	4.6	6.5	10.4
1	1	0	4.3	5.8	7.8	11.7
1	1	1	4.5	6.5	8.8	13.0

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Title	PEIe 0-7 Gen 4 Re-driver	
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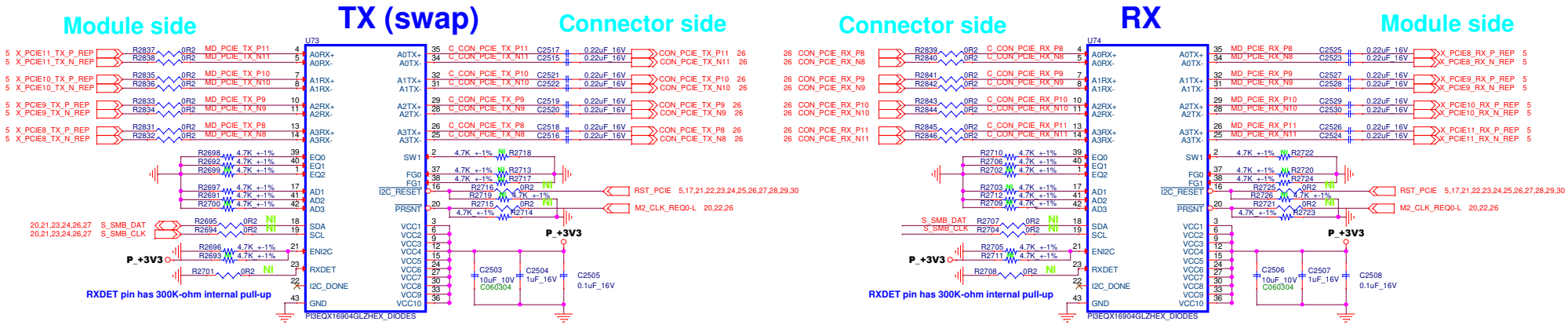
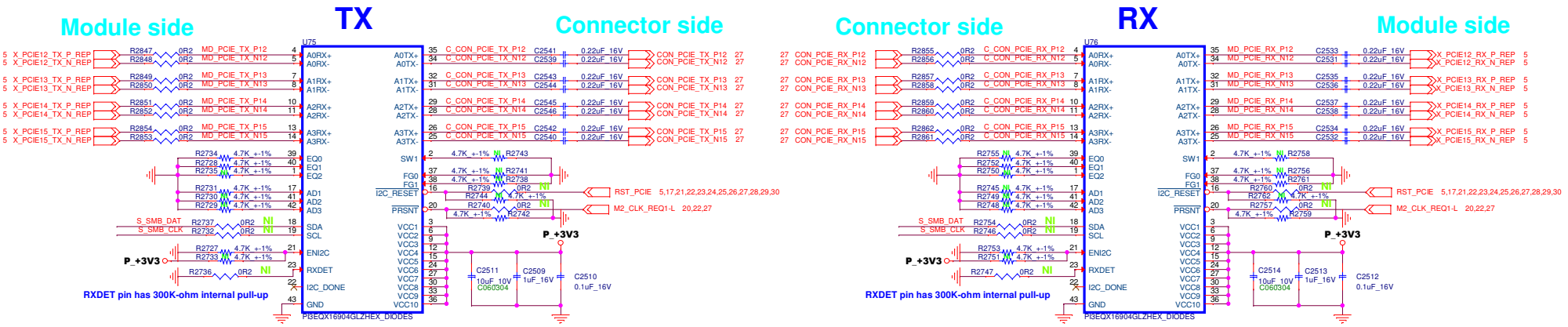
PCIe x4 M.2 slot1 (PCIe 8-11) re-driver



PCIe x4 M.2 slot2 (PCIe 12-15) re-driver



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Title	PEIe 8-15 Gen 4 Re-driver	
Size: Custom	Document Number: COM-HPC Server Base	Rev: A1
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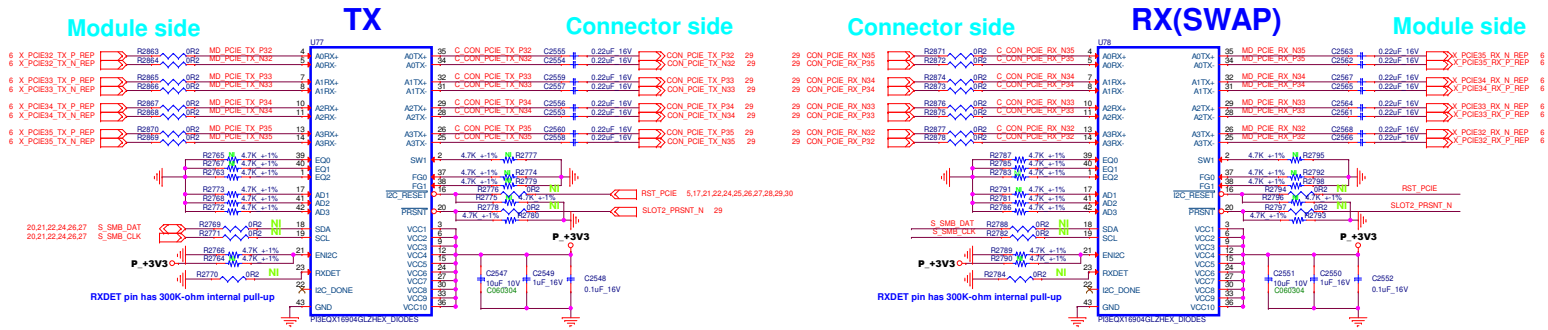
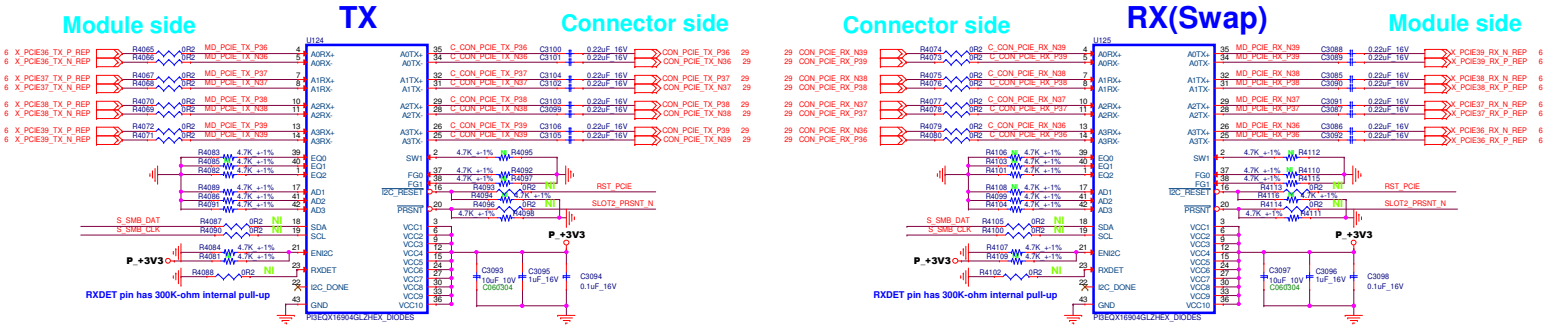
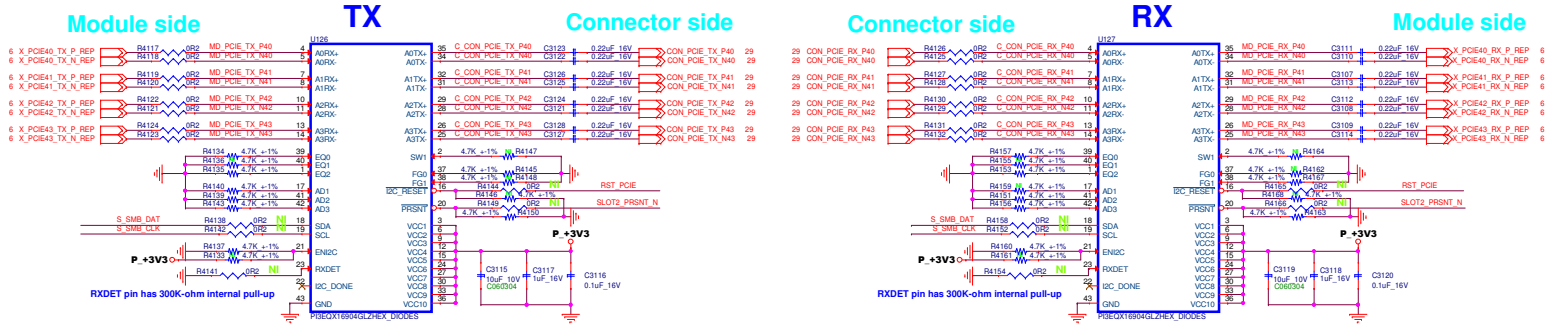
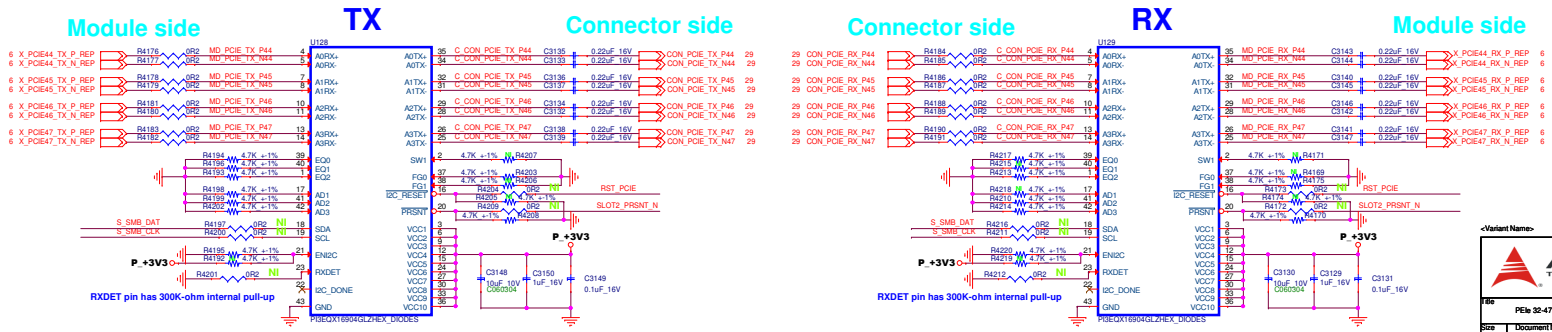
PCIe x16 Slot 2 (PCIe 32-47) Gen4 re-driver









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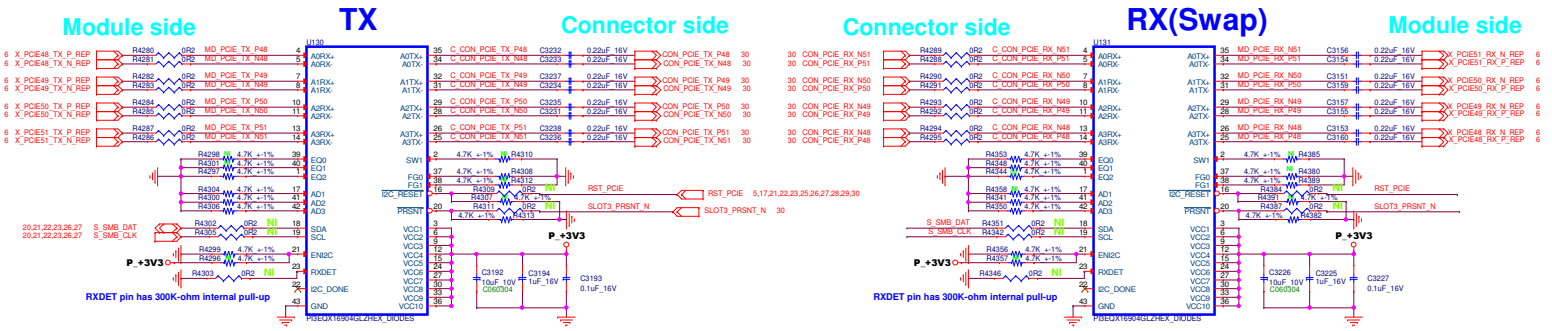
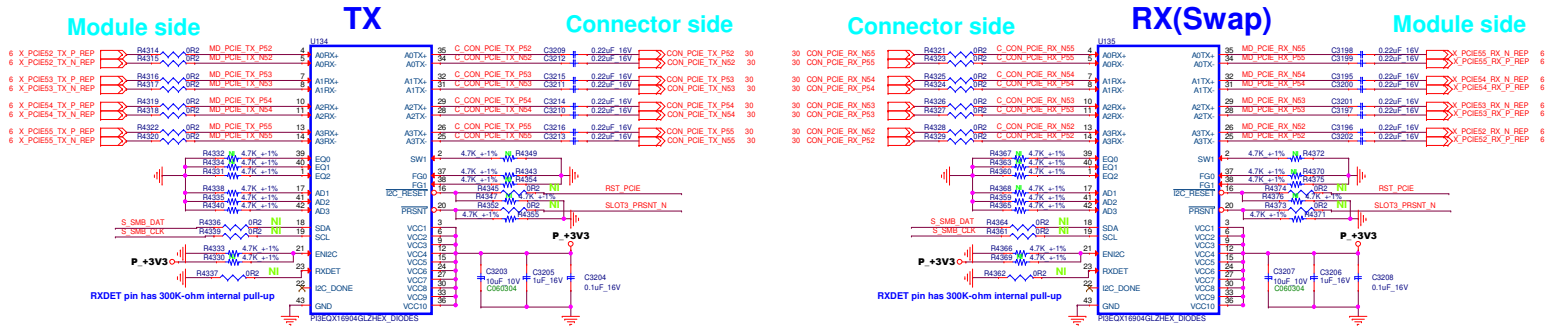
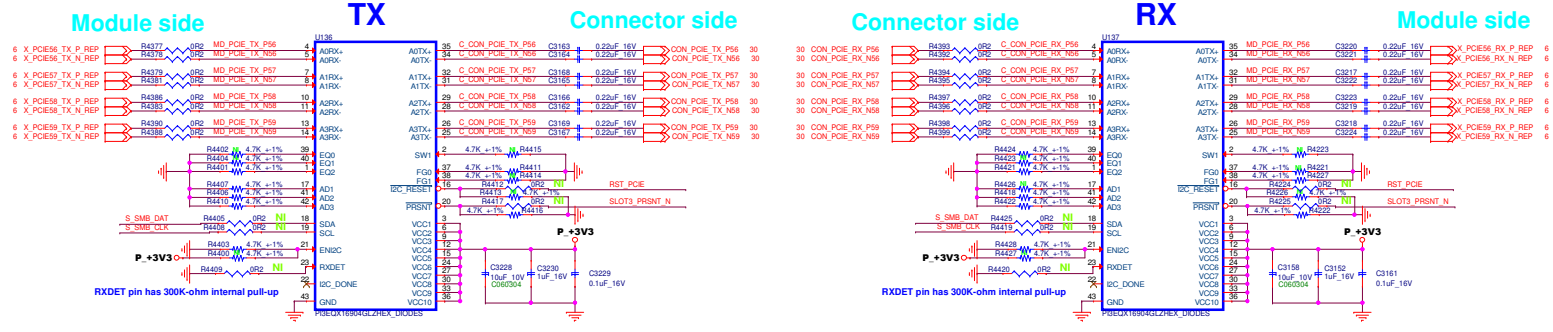
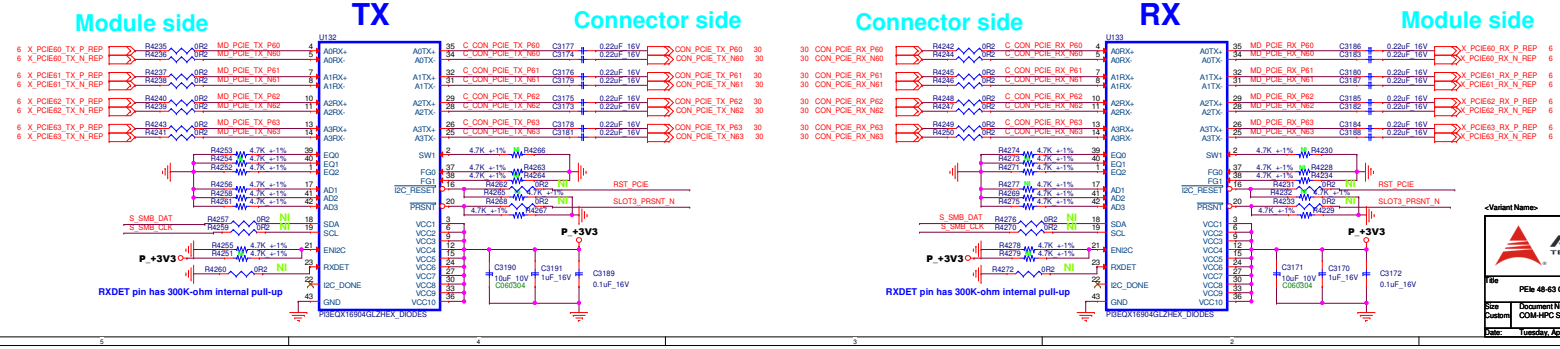
PCIe x16 Slot 2 (PCIe 48-63) re-driver









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Title: PEIe 48-63 Gen 4 Re-driver

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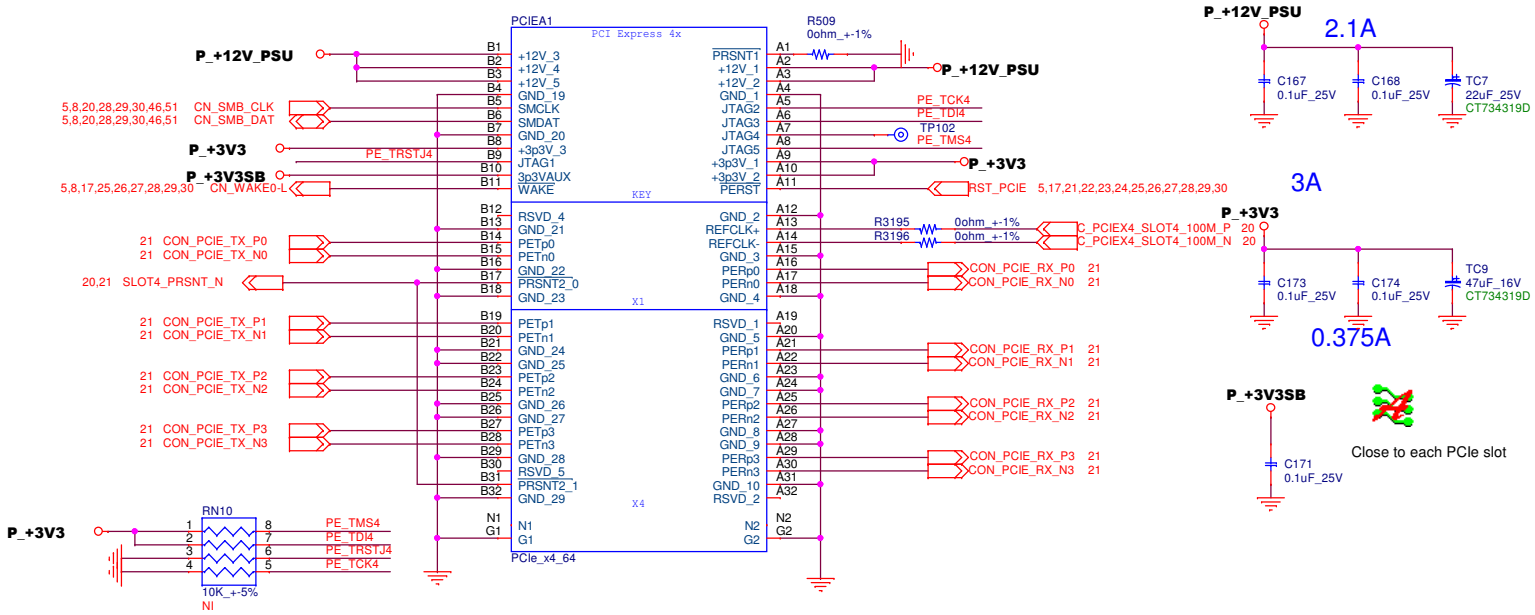
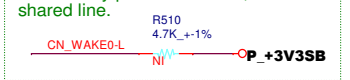
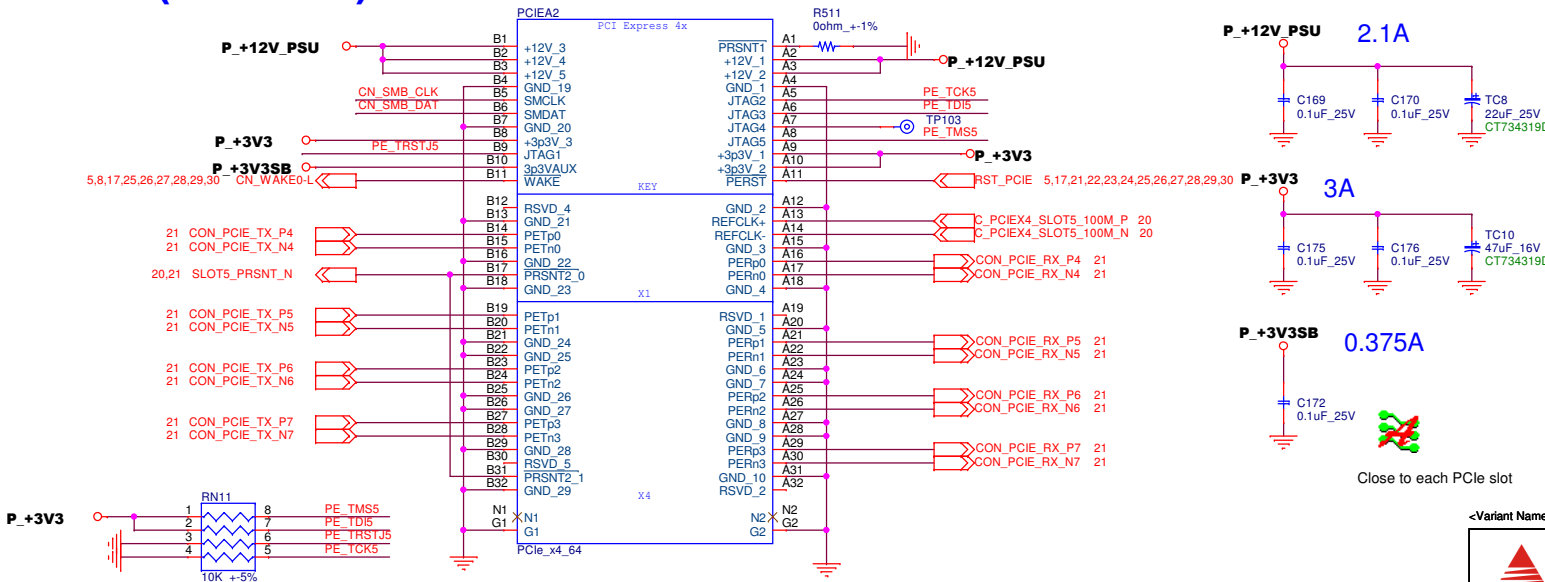
PCIe x4 Slot (PCIe 0-3)



WAKE0# is asserted by the slot card to cause COM Express Module wake-up at Module pin B66. This is an open-drain signal. It is an input to the Module and is pulled up on the Module. Other WAKE0# ources may pull this line low; it is a shared line.



PCIe x4 Slot (PCIe 4-7)



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Title	PCIe x4 Slot (PCIe 0-3, 4-7)	
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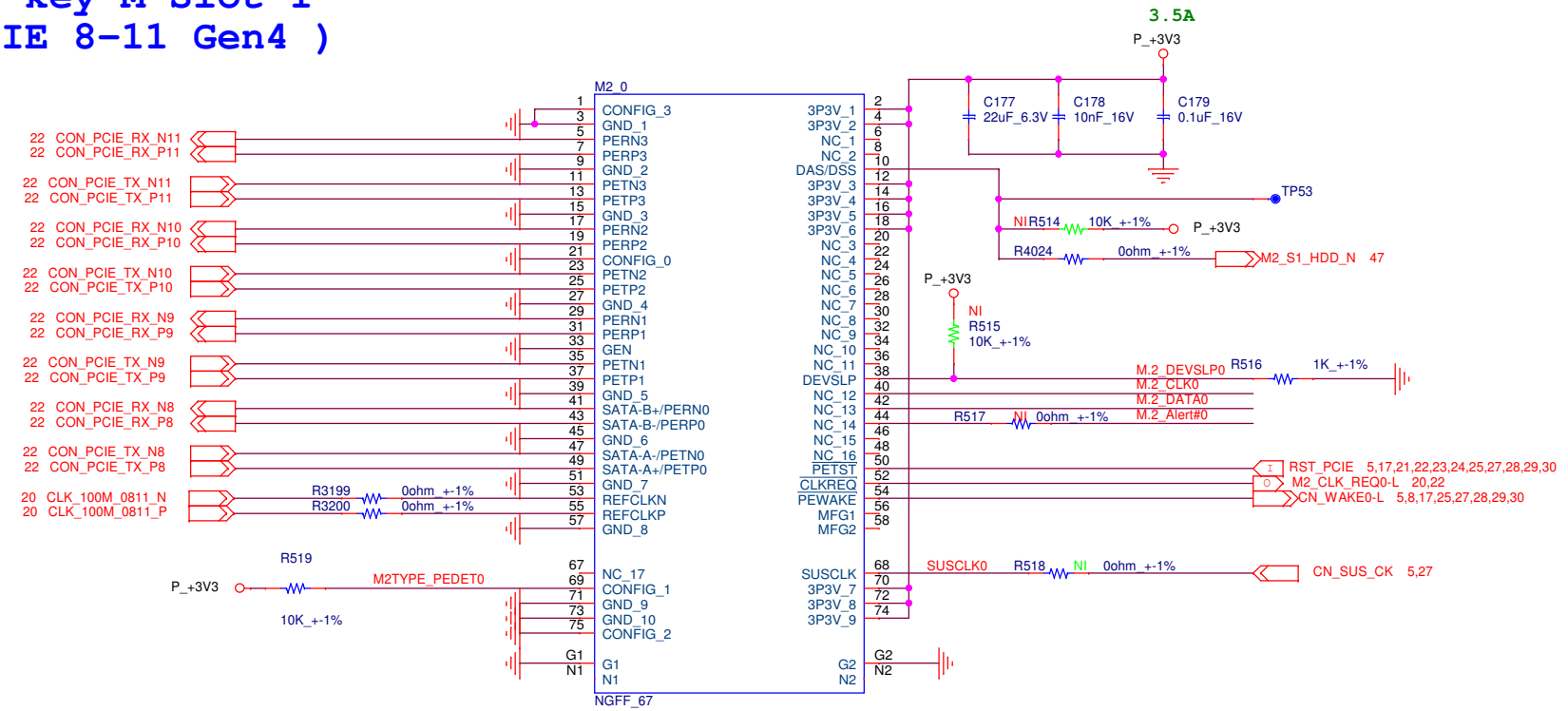
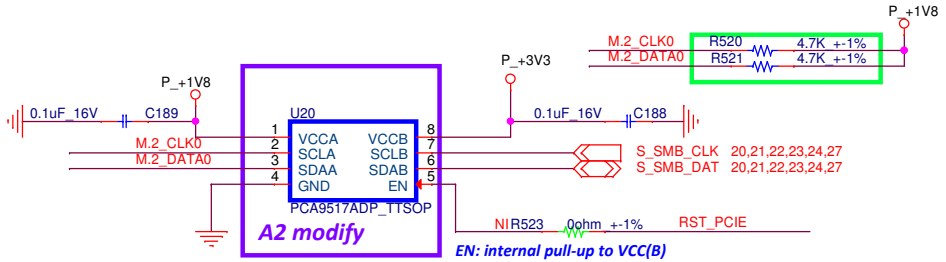
M.2 key-M Slot 1 (PCIE 8-11 Gen4)





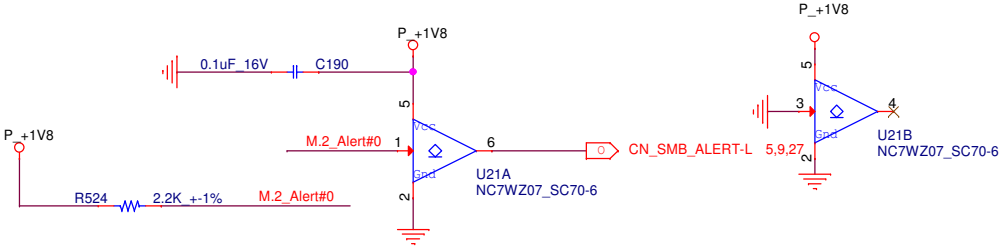


Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

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Title	M.2 key-M Slot (PCIe 8-11)	
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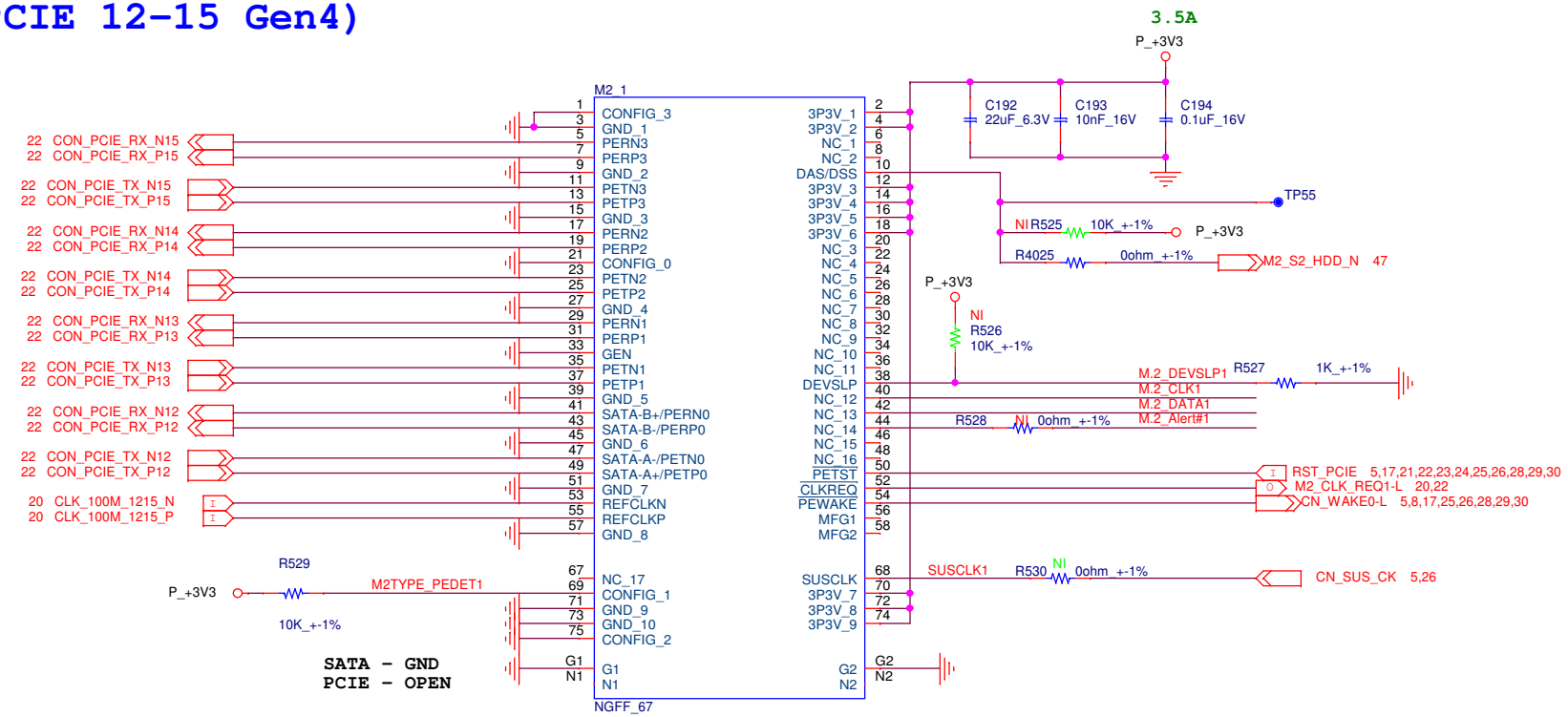
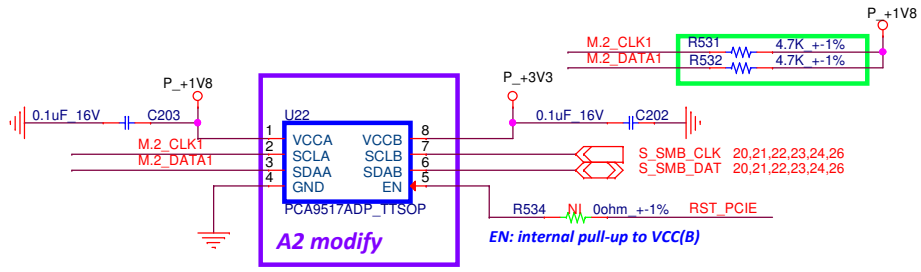
M.2 key-M Slot 2 (PCIE 12-15 Gen4)





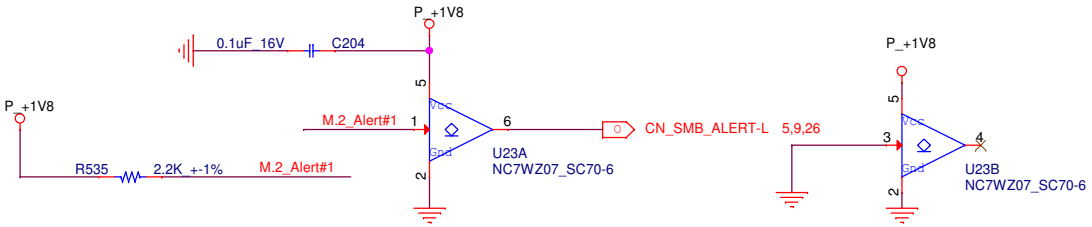


Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

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Title	M.2 key-M Slot (PCIe 12-15)	
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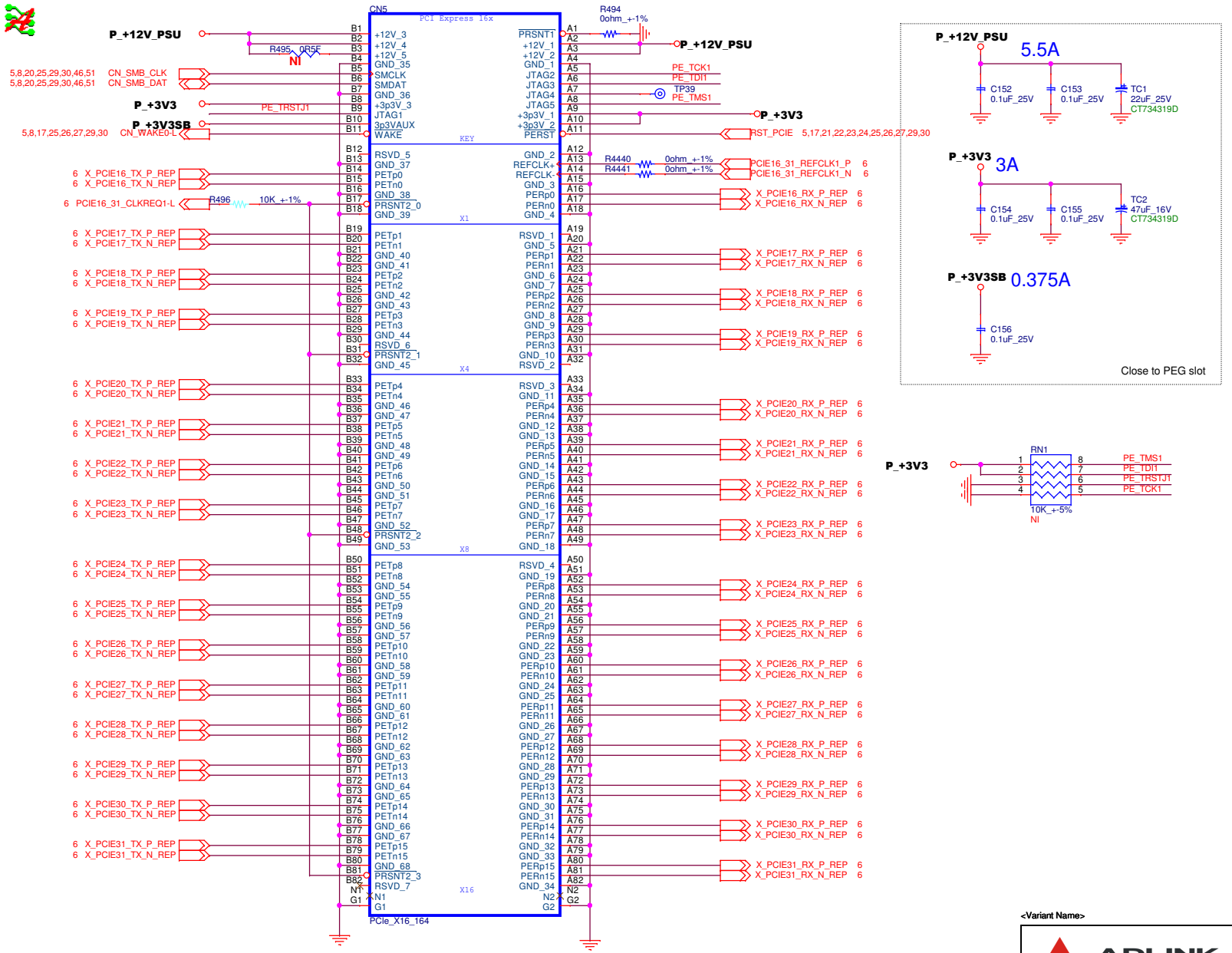
PCIe x16 Slot1 (PCIe 16-31)



<Variant Name>

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Title	PCIe x16 Slot1 (PCIe 16-31)	
Size: Custom	Document Number: COM-HPC Server Base	Rev: A1
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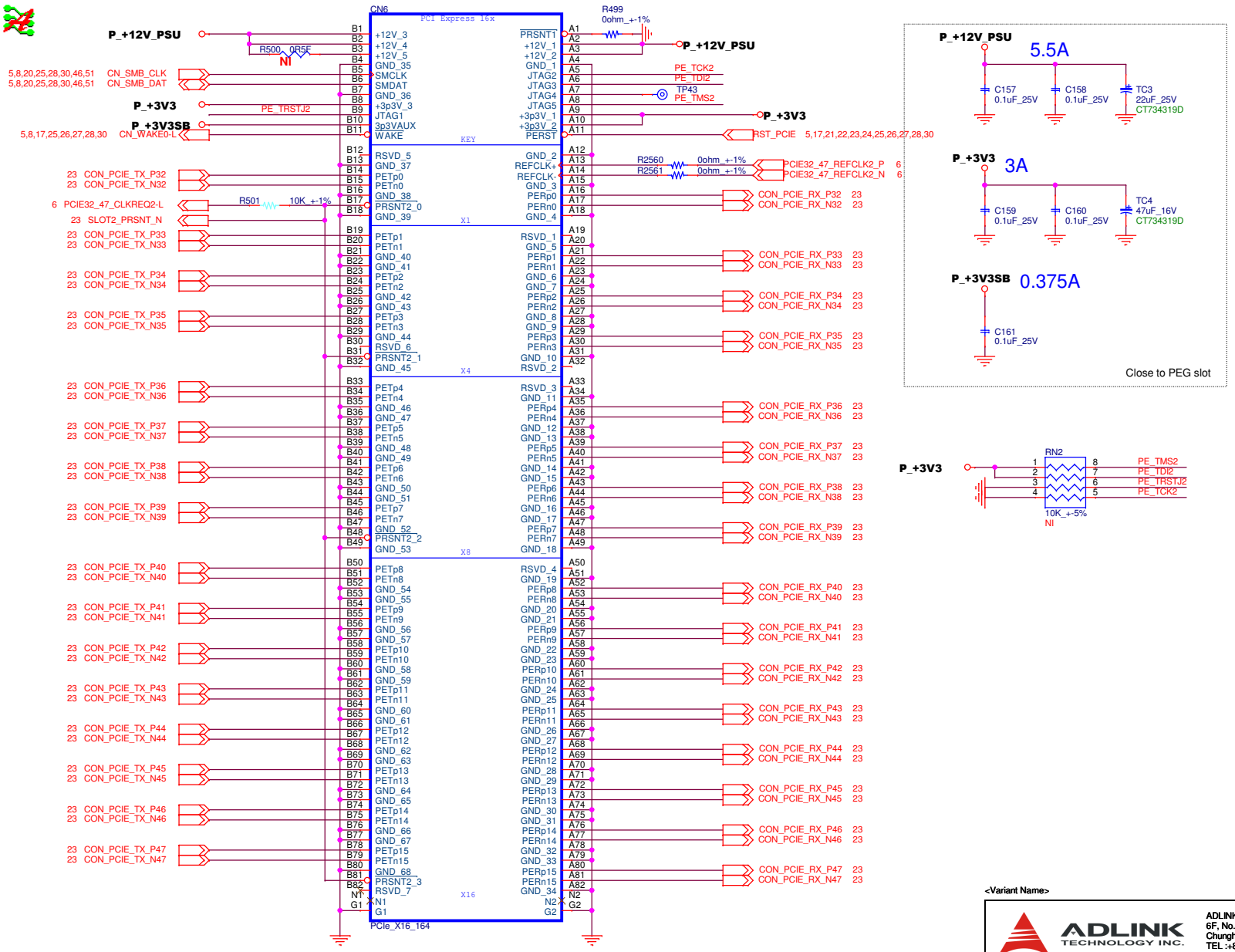
PCIe x16 Slot (PCIe 32-47)



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Title	PCIe x16 Slot (PCIe 32-47)	
Size: Custom	Document Number: COM-HPC Server Base	Rev: A1
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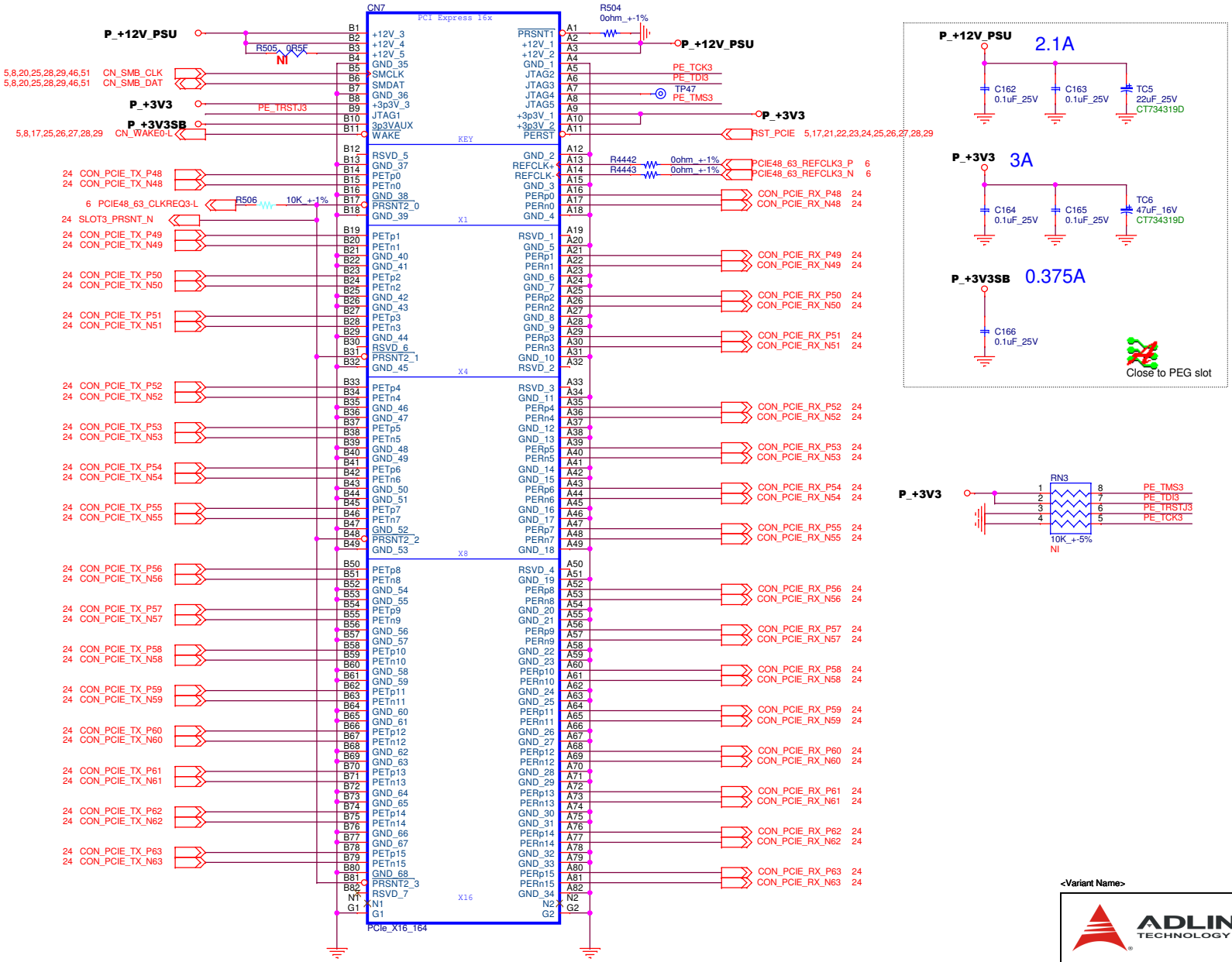
PCIe x8 Slot3 (PCIe 48-63)



<Variant Name>

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Title	PCIe x16 Slot 3 (48-63)	
Size: Custom	Document Number: COM-HPC Server Base	Rev: A1
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Title

Size	Document Number	Rev
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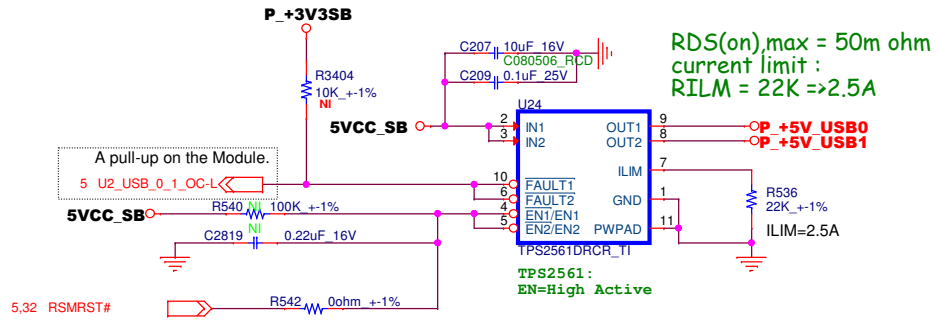

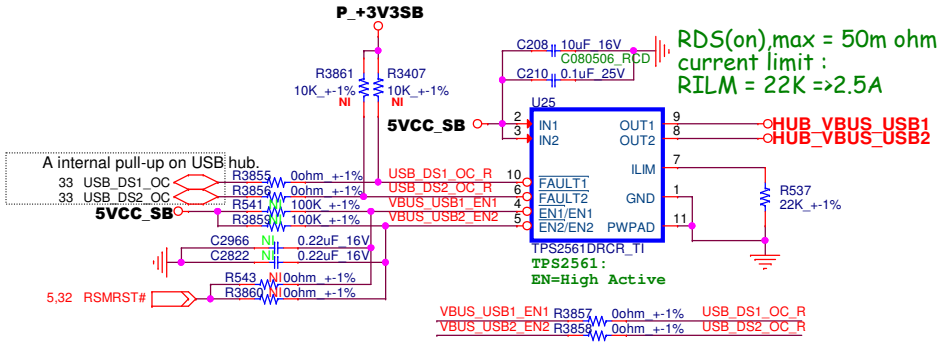

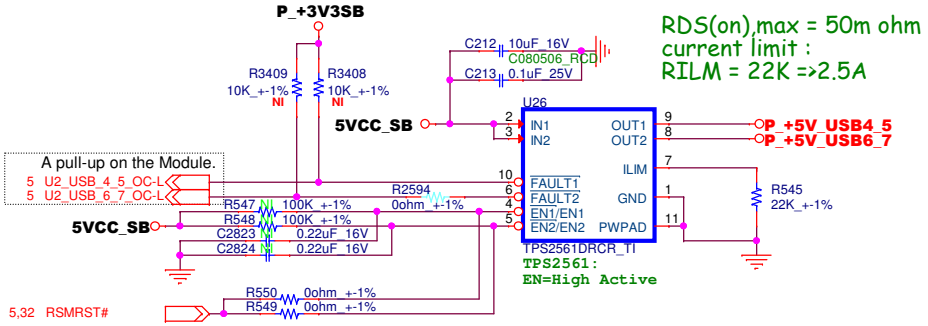

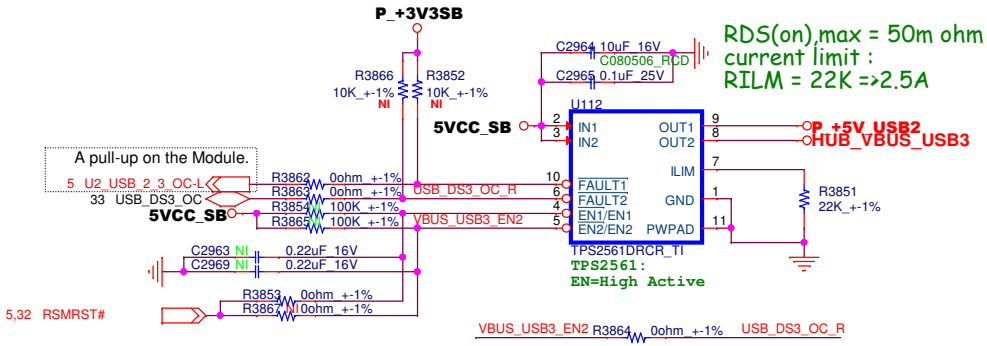

DEVICE[1]	AMBIENT TEMPERATURE [2]	ENABLE	SON [3] (DRC)	MARKING	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT PER CHANNEL
TPS2560	–40°C to 85°C	Active low	TPS2560DRC	2560	2.5 A
TPS2561		Active high	TPS2561DRC	2561	

DESIRED NOMINAL CURRENT LIMIT	IDEAL RESISTOR	CLOSEST 1% RESISTOR	1% LOW RESISTOR TOLERANCE	1% HIGH RESISTOR TOLERANCE	IOS ACTUAL LIMITS			
					MIN	NOM	MAX	UNIT
300 mA	186.7 kΩ	187 kΩ	185.1 kΩ	188.9 kΩ	241.6	299.5	357.3	mA
400 mA	140.0 kΩ	140 kΩ	138.6 kΩ	141.4 kΩ	328.0	400.0	471.4	mA
600 mA	93.3 kΩ	93.1 kΩ	92.2 kΩ	94.0 kΩ	504.6	601.5	696.5	mA
800 mA	70.0 kΩ	69.8 kΩ	69.1 kΩ	70.5 kΩ	684.0	802.3	917.6	mA
1000 mA	56.0 kΩ	56.2 kΩ	55.6 kΩ	56.8 kΩ	859.9	996.4	1129.1	mA
1200 mA	46.7 kΩ	46.4 kΩ	45.9 kΩ	46.9 kΩ	1052.8	1206.9	1356.3	mA
1400 mA	40.0 kΩ	40.2 kΩ	39.8 kΩ	40.6 kΩ	1225.0	1393.0	1555.9	mA
1600 mA	35.0 kΩ	34.8 kΩ	34.5 kΩ	35.1 kΩ	1426.5	1609.2	1786.2	mA
1800 mA	31.1 kΩ	30.9 kΩ	30.6 kΩ	31.2 kΩ	1617.3	1812.3	2001.4	mA
2000 mA	28.0 kΩ	28 kΩ	27.7 kΩ	28.3 kΩ	1794.7	2000.0	2199.3	mA
2200 mA	25.5 kΩ	25.5 kΩ	25.2 kΩ	25.8 kΩ	1981.0	2196.1	2405.3	mA
2400 mA	23.3 kΩ	23.2 kΩ	23.0 kΩ	23.4 kΩ	2188.9	2413.8	2633.0	mA
2600 mA	21.5 kΩ	21.5 kΩ	21.3 kΩ	21.7 kΩ	2372.1	2604.7	2831.9	mA
2800 mA	20.0 kΩ	20 kΩ	19.8 kΩ	20.2 kΩ	2560.4	2800.0	3034.8	mA

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Title: USB Power Switch

Size: B | Document Number: COM-HPC Server Base | Rev: A1

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USB3.2 Gen2 Hub

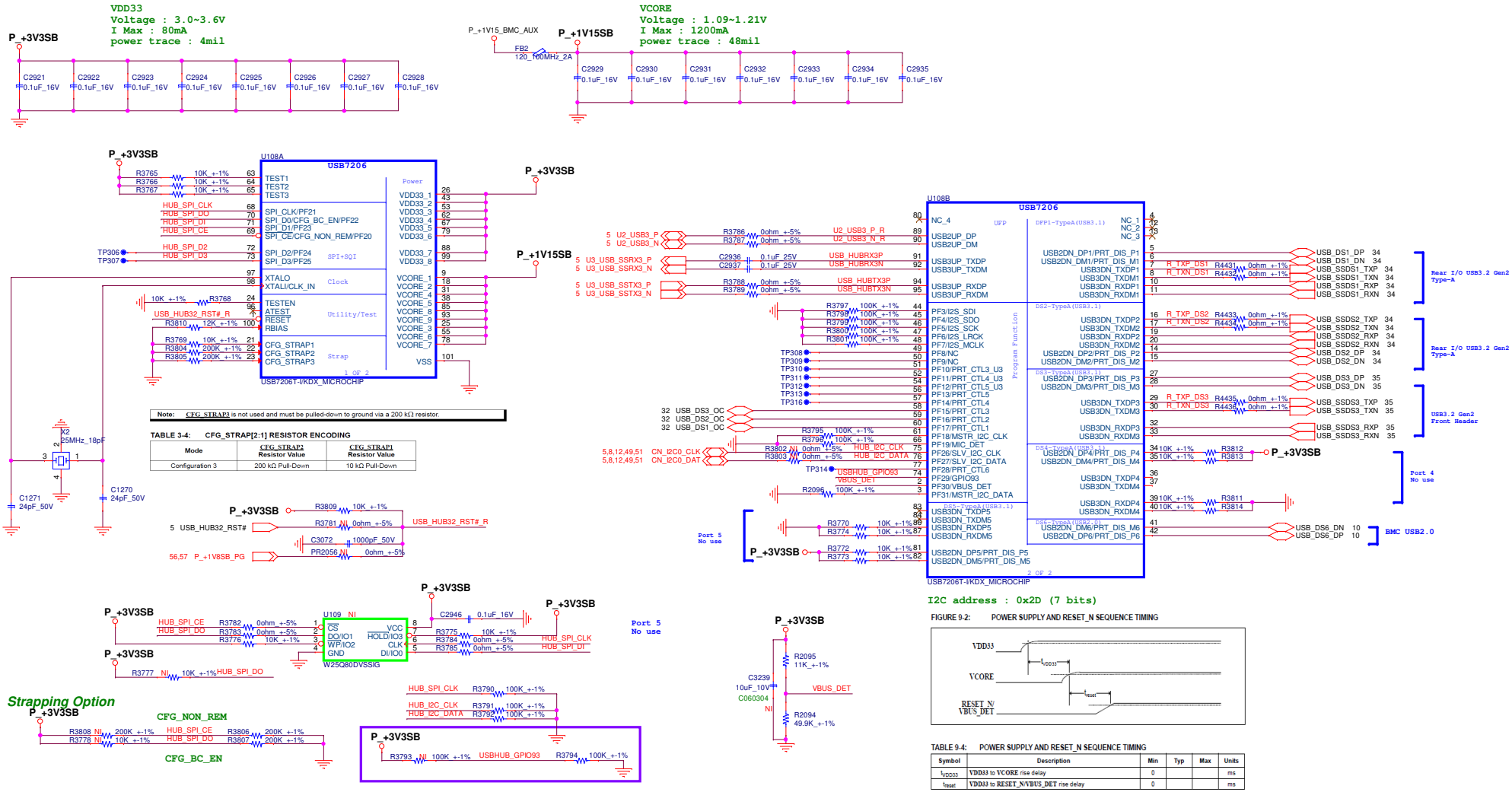

TABLE 3-3: CFG_BC_EN RESISTOR ENCODING

CFG_BC_EN Resistor Value	Setting
200 kΩ Pull-Down	Battery charging not enable on any port
200 kΩ Pull-Up	BC1.2 DCP and CDP battery charging enabled on Port 1
10 kΩ Pull-Down	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2
10 kΩ Pull-Up	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3
10 Ω Pull-Down	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3, 4
10 Ω Pull-Up	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3, 4, 5, 6

TABLE 10-5: CFG_NON_REM

Setting	Effect
200 kΩ pull-down to GND	All ports removable (Recommended for most USB7206applications)
200 kΩ pull-up to 3.3V	Port 1 is non-removable. Only a valid selection if Port 1 is connected directly to an embedded USB device.
10 kΩ pull-down to GND	Ports 1 and 2 are non-removable. Only a valid selection if Ports 1 and 2 are connected directly to embedded USB devices.
10 kΩ pull-up to 3.3V	Ports 1, 2, and 3 are non-removable. Only a valid selection if Ports 1, 2, and 3 are connected directly to embedded USB devices.
10 kΩ pull-down to GND	Ports 1, 2, 3, and 4 are non-removable. Only a valid selection if ports 1, 2, 3, and 4 are connected directly to embedded USB devices.

TABLE 9-4: POWER SUPPLY AND RESET_N SEQUENCE TIMING

Symbol	Description	Min	Typ	Max	Units
t_{VDD33}	VDD33 to VCORE rise delay	0			ms
t_{reset}	VDD33 to RESET_N/VBUS_DET rise delay	0			ms

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Block: USB3.2 Gen2 Hub
Size: Custom
Project Name: COM-HPC Server Base
Rev: A1
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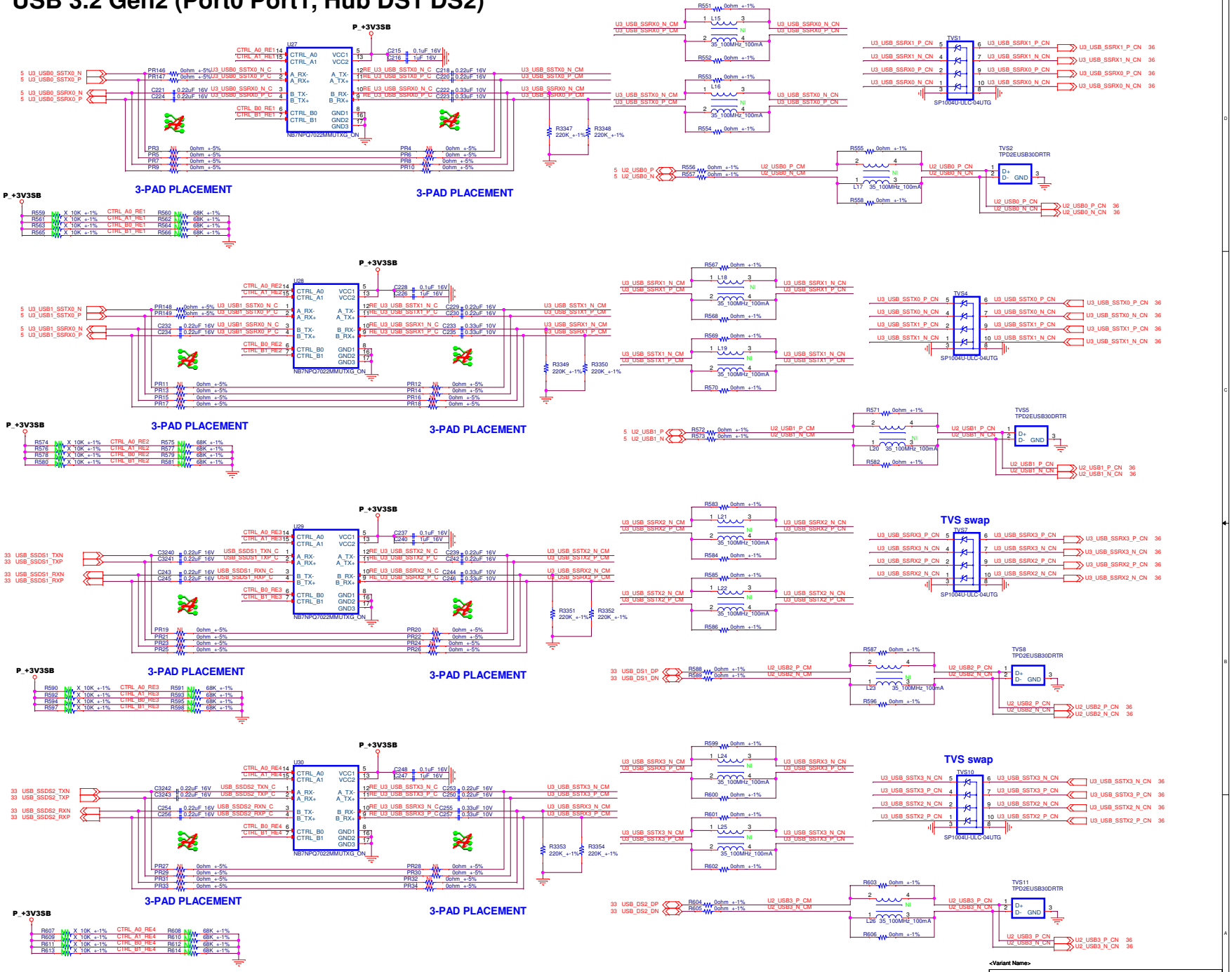
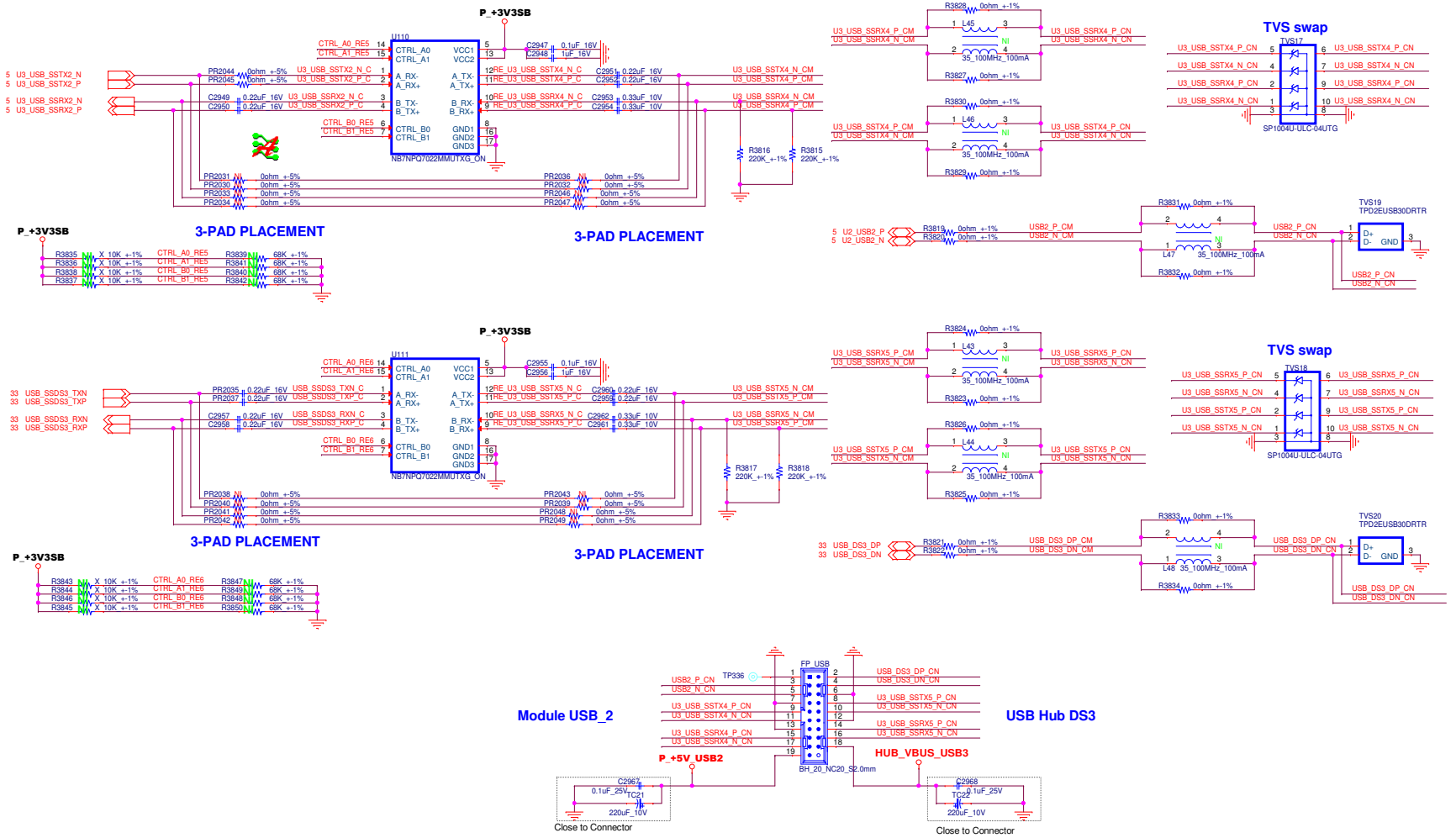
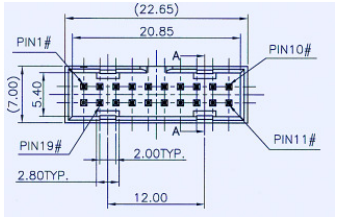
USB 3.2 Gen2 (Port0 Port1, Hub DS1 DS2)

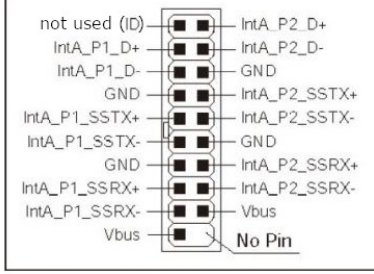


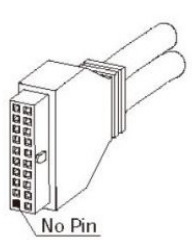
Frontpanel USB 3.2 Gen2 redriver (Port2, Hub DS3)





Motherboard - NORMAL	Case Connector
Front panel USB3.0 connector	USB3.0 connector





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Title		
USB3.2 Gen2 Front Header		
Size: C	Document Number: COM-HPC Server Base	Rev: A1
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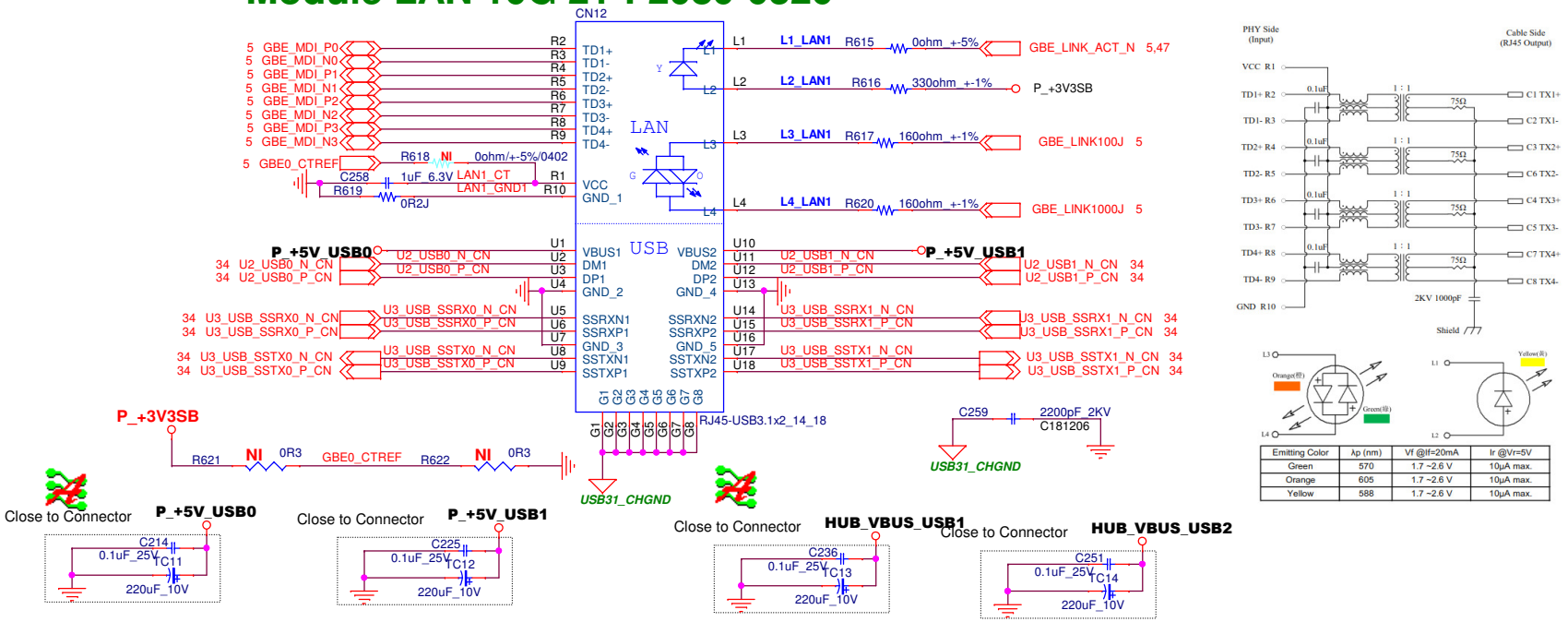
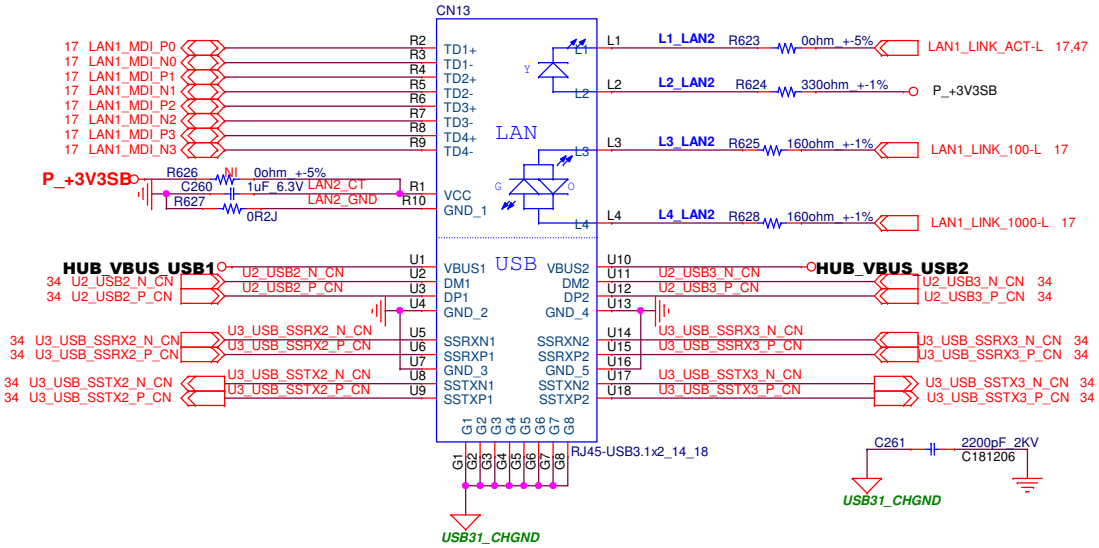
Module LAN 10G 21-F2080-0320



Emitting Color	λp (nm)	Vf @If=20mA	Ir @Vr=5V
Green	570	1.7 ~2.6 V	10μA max.
Orange	605	1.7 ~2.6 V	10μA max.
Yellow	588	1.7 ~2.6 V	10μA max.

BMC Dedicate NIC 100M



ACT : BLINK (Yellow)
Speed 100 : Green
Speed 1G : Orange

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Block: RJ45+2x1 USB typeA x2		
Size: B	Project Name: COM-HPC Server Base	Rev: A1
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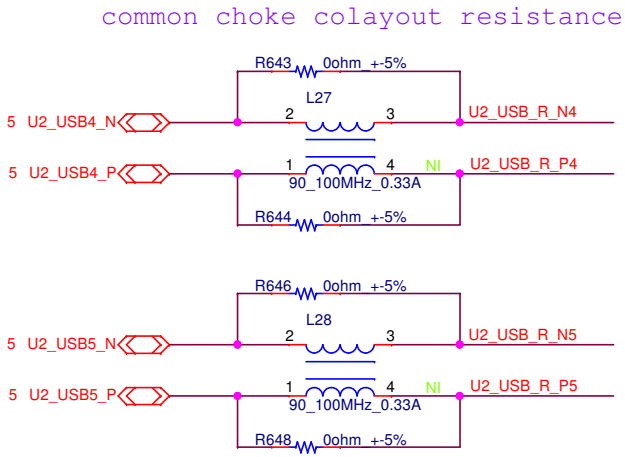
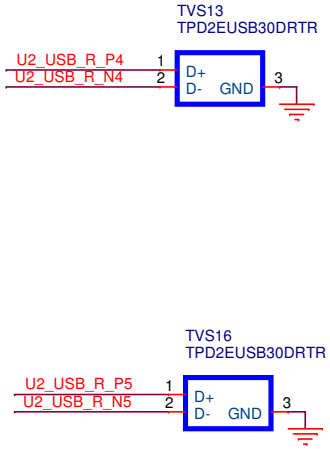
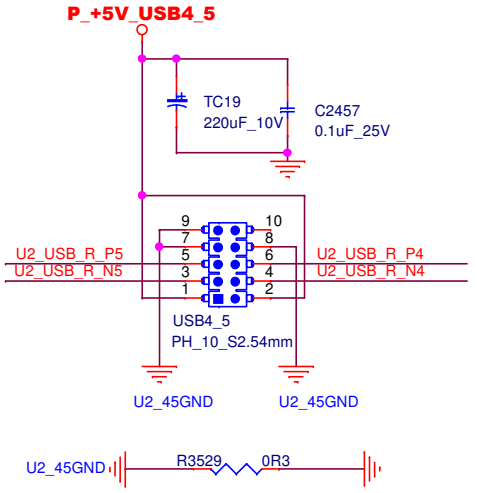
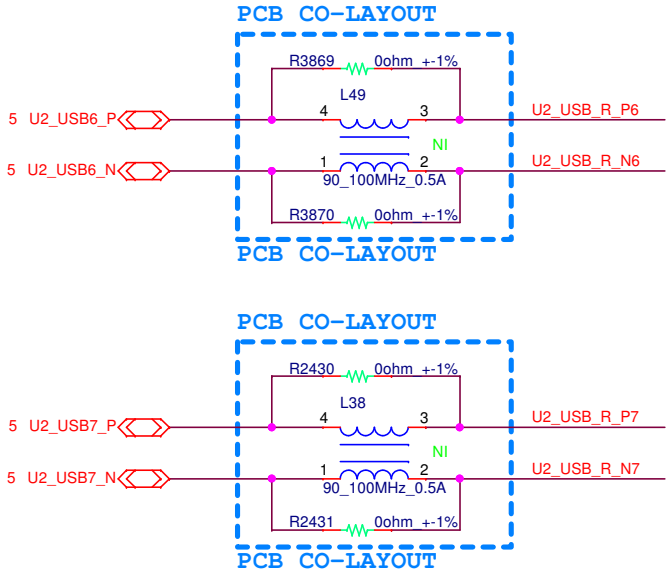
USB2.0 pin header (Module Port 4-5)

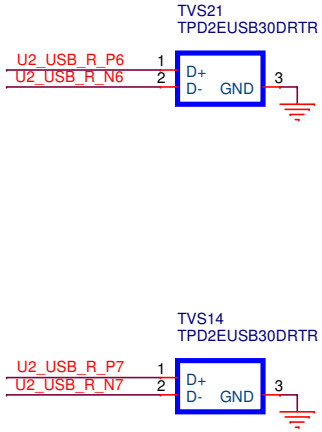


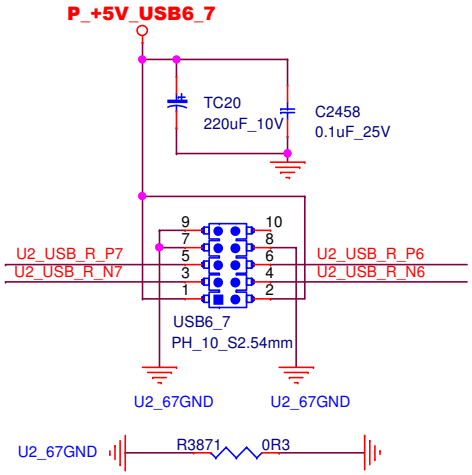




USB2.0 pin header (Module Port 6-7)







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Title	USB2.0 (Port4-7) pin header	
Size: Custom	Document Number: COM-HPC Server Base	Rev: A1
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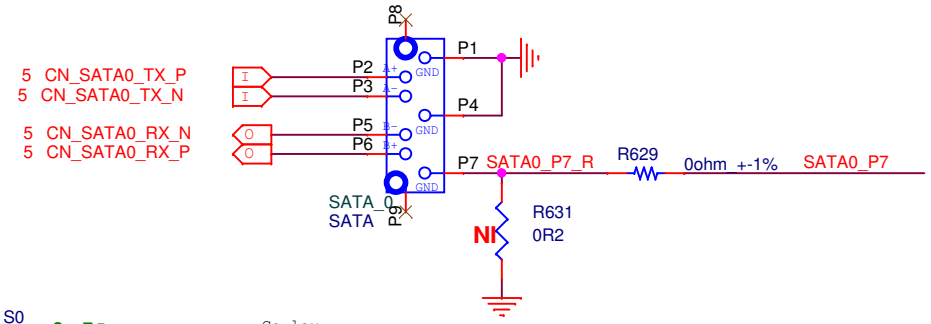
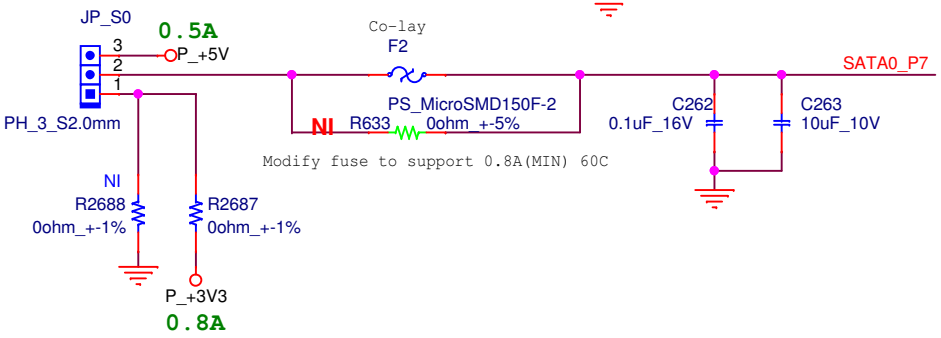
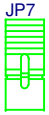
SATA 0 Gen3





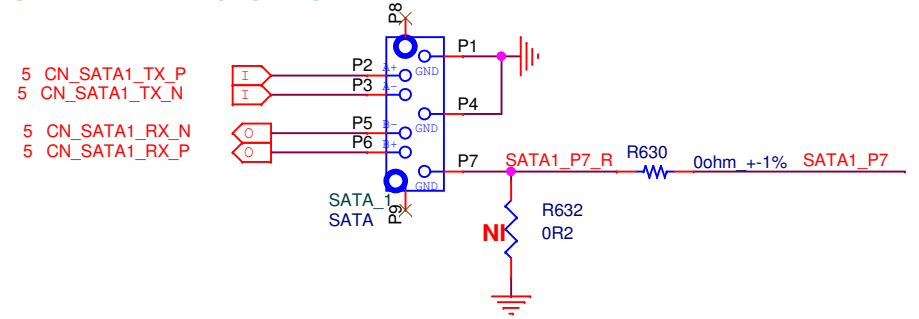
JP7

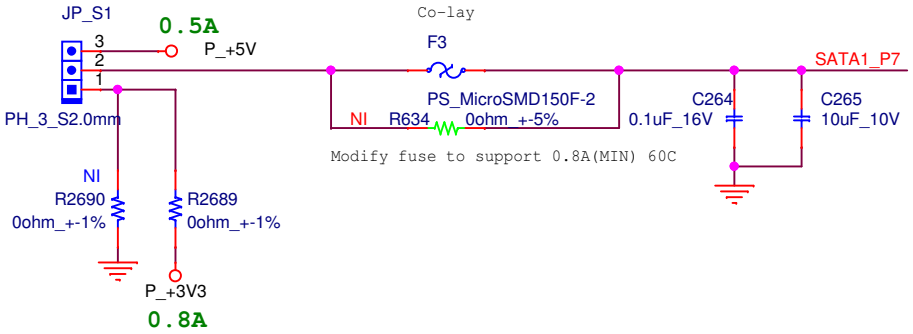


MINI-JUMP_2_S2.0mm

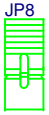
JPS3P1_SATA1 DOM Power	
1-2	3.3V
2-3	5V
NC	Default

SATA 1 Gen3



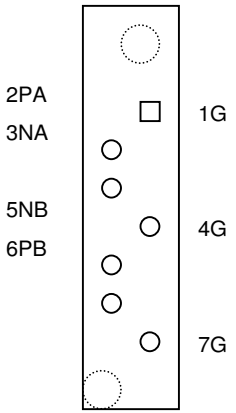


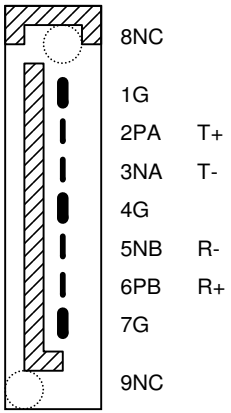
JP8



MINI-JUMP_2_S2.0mm

JPS4P1_SATA2 DOM Power	
1-2	3.3V
2-3	5V
NC	Default





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Title: SATA port1/2 (SATA DOM)

Size: A4 | Document Number: COM-HPC Server Base | Rev: A1

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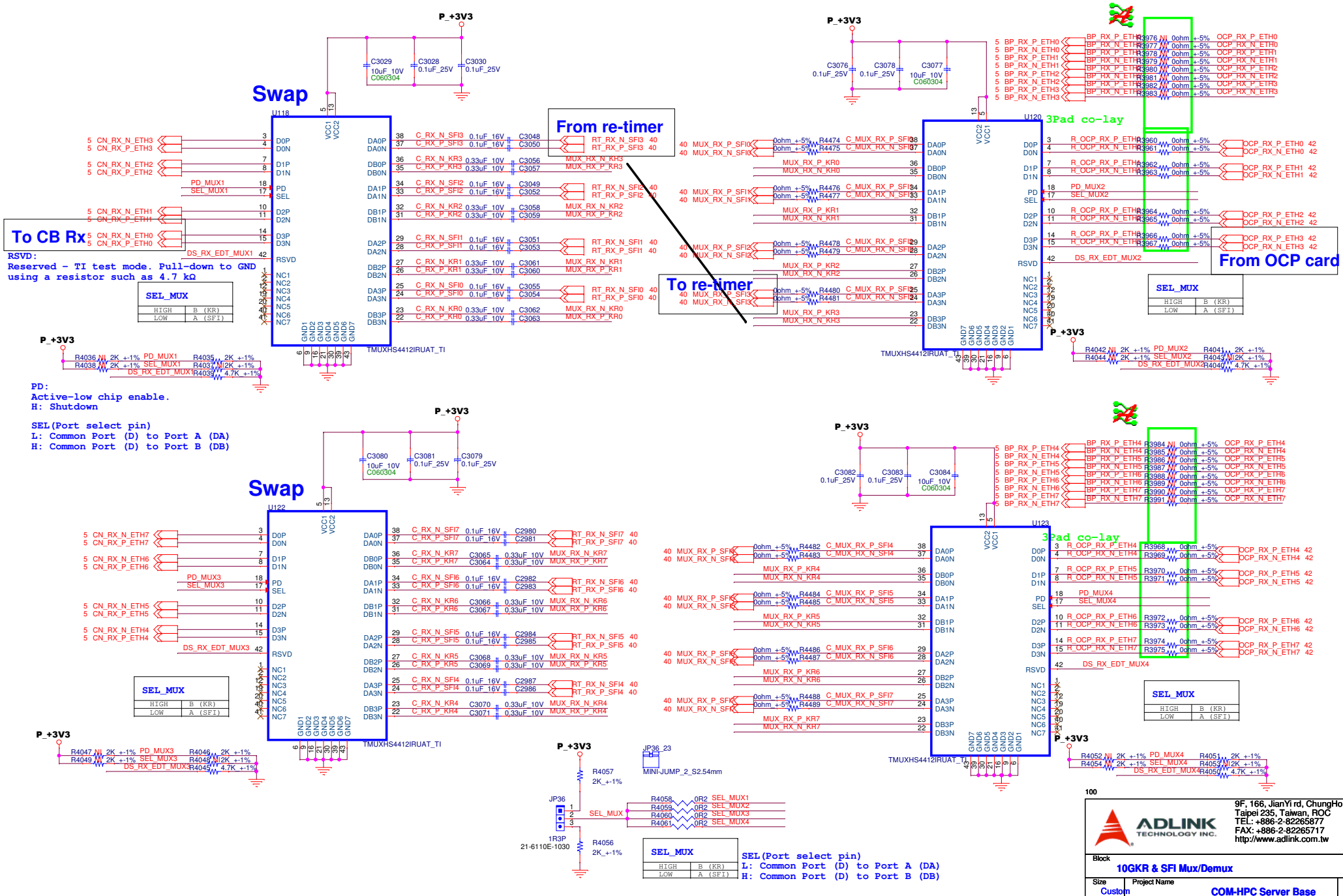
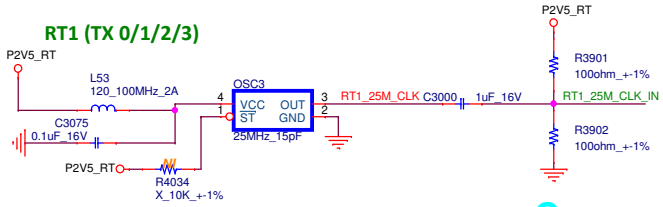
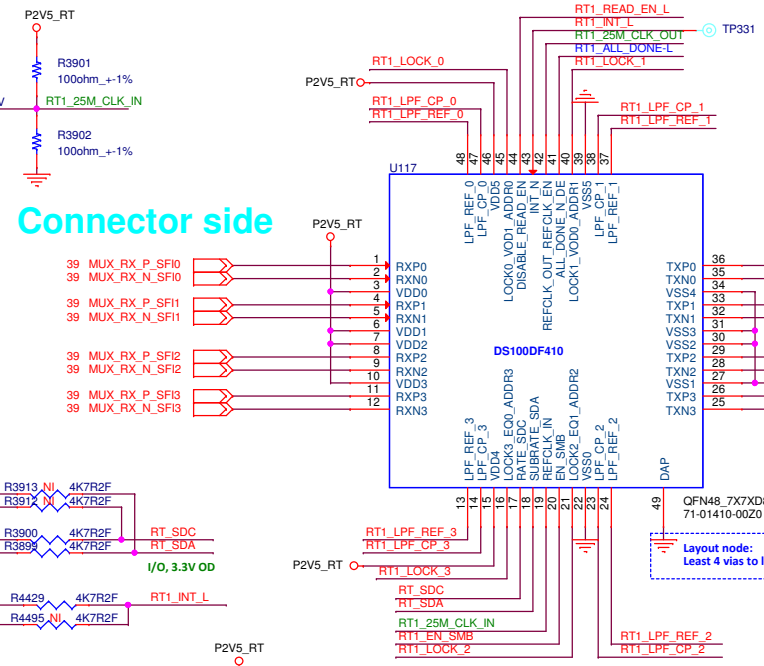
10GKR & SFI Mux/Demux



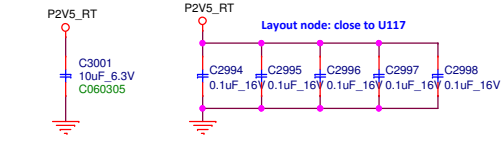
RT1 (TX 0/1/2/3)



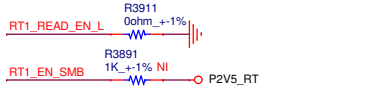
Connector side



Module side

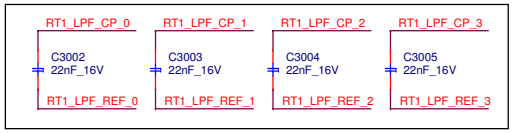


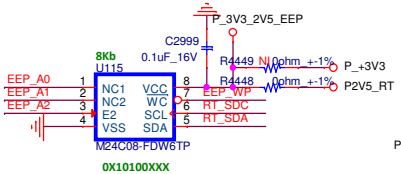
Input is 2.5 V, a transition from high to low starts the load from the external EEPROM.
The READ_EN pin must be tied low when in SMBus slave mode

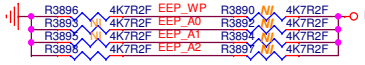


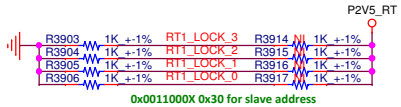
EN_SMB = High for slave mode
EN_SMB = Float for master mode
Tie READ_EN pin low for SMBus slave mode.

Layout node: close to U117



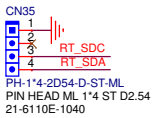


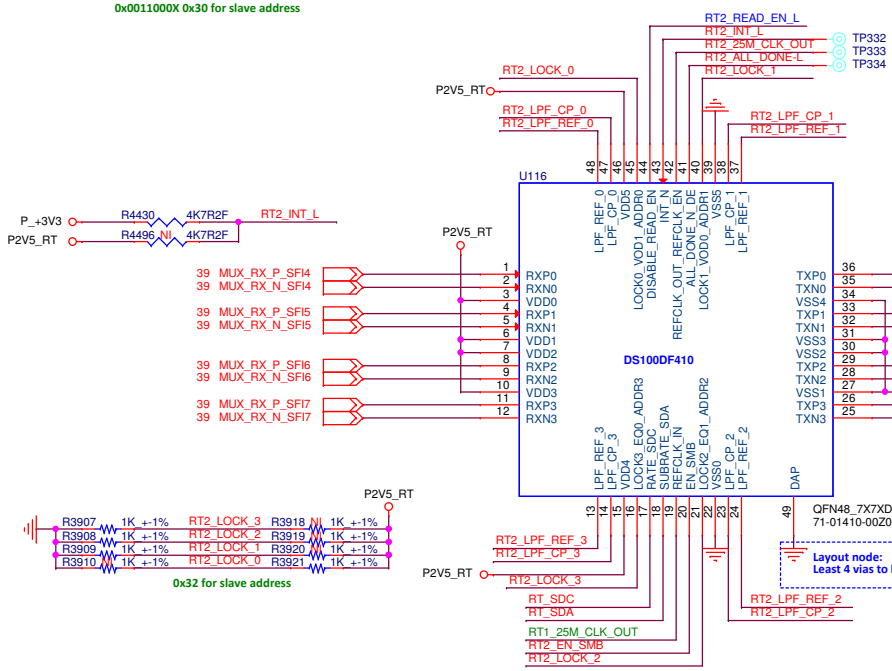


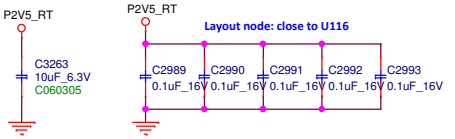


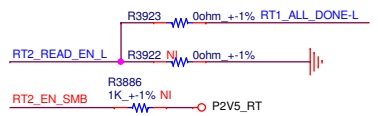
RT2 (TX 4/5/6/7)

External SMBus Connector



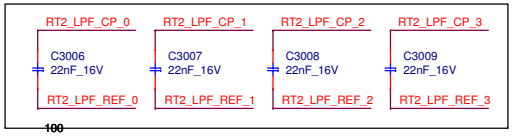






EN_SMB = High for slave mode
EN_SMB = Float for master mode
Tie READ_EN pin low for SMBus slave mode.

Layout node: close to U116



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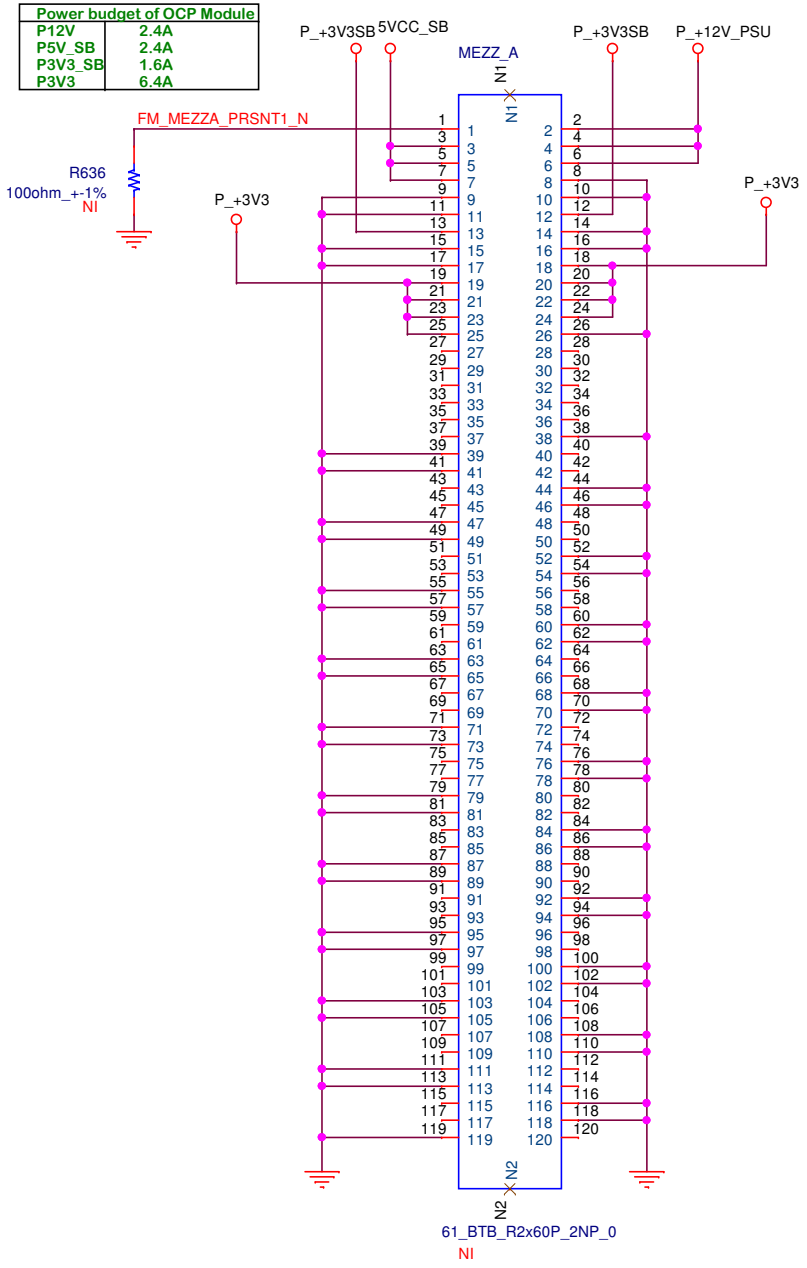
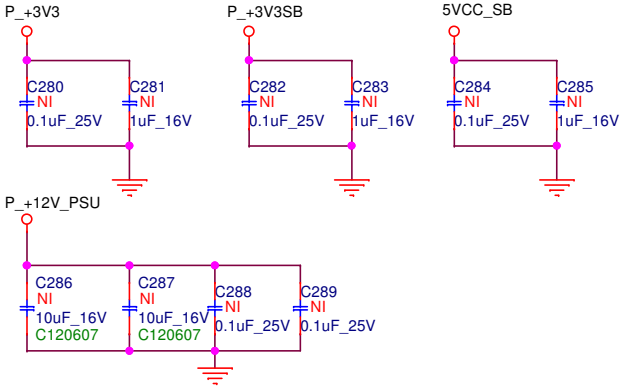
Block	SFI0,1,2,3 RX Re-timmer	
Size: Custom	Project Name: COM-HPC Server Base	Rev: A1
Date: Tuesday, April 11, 2023	Sheet 40 of 66	

Power budget of OCP Module	
P12V	2.4A
P5V_SB	2.4A
P3V3_SB	1.6A
P3V3	6.4A

0.8A/PIN





<Variant Name>

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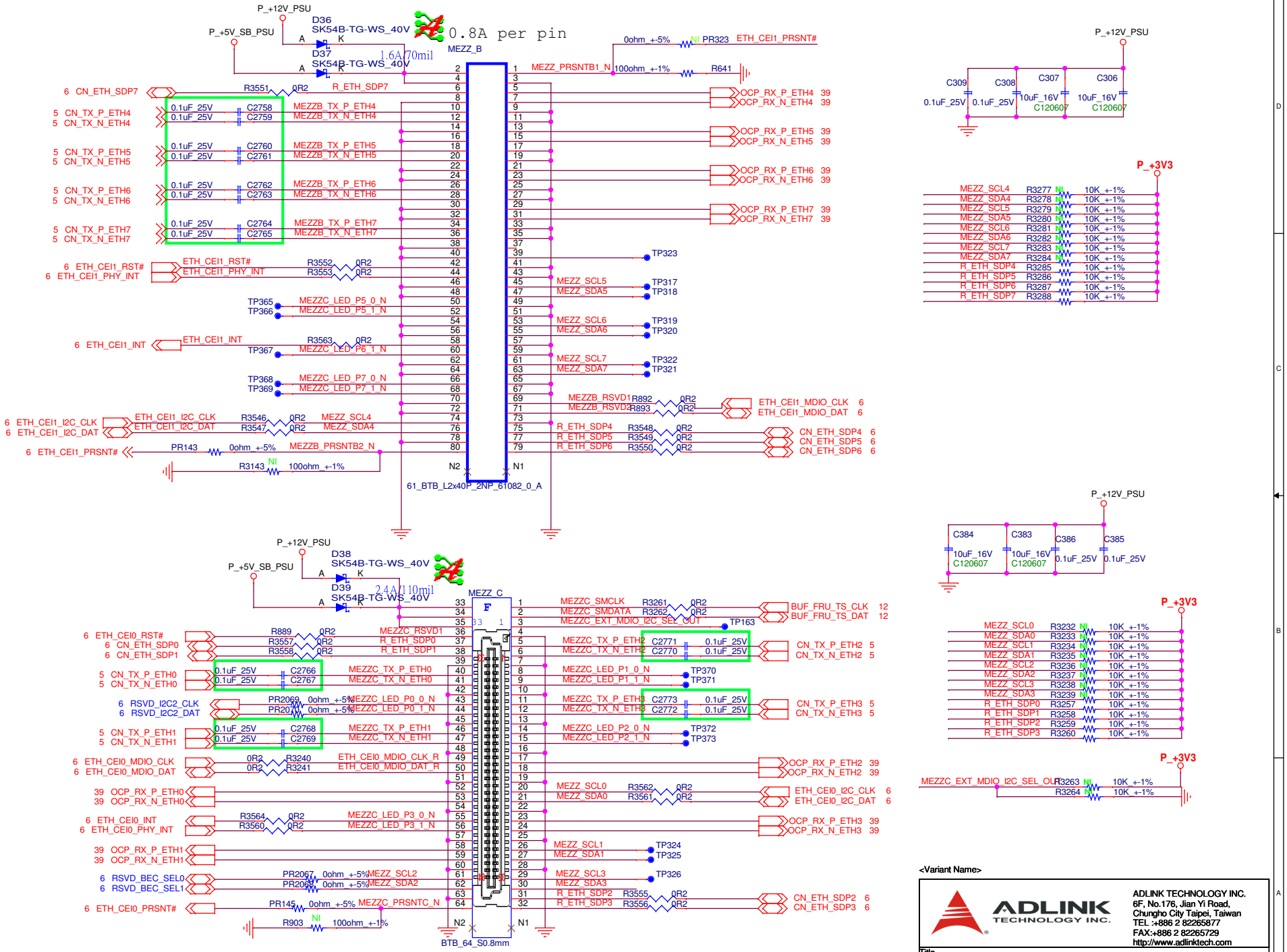
Title			
OCP Mezz CNA			
Size: Custom	Document Number: COM-HPC Server Base		Rev: A1
Date: Tuesday, April 11, 2023		Sheet 41 of 66	



<Variant Name>

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Title	OCP_Mezz CNB/CNC	
Size: Custom	Document Number: COM-HPC Server Base	Rev: A1
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Molude UART0 with Serial Port DB9

Reseverd Close to Q7 Q8

MUX_SER0_TX	R657 NI	0ohm +-1%	CN_SER0_TX_2
MUX_SER0_RX	R658 NI	0ohm +-1%	CN_SER0_RX_2
MUX_SER0_RTS_L	R659 NI	0ohm +-1%	CN_SER0_RTS_L_2
MUX_SER0_CTS_L	R660 NI	0ohm +-1%	CN_SER0_CTS_L_2

5VCC_SB
P_+3V3SB
C331 0.1uF_25V
R653 4.7K_+-1%
CN_SER0_TX_1
U33 74AHC1G14_SOT23-5
CN_SER0_TX_2
MUX_SER0_TX
Q7 NX7002AK_300mA/60V
R654 4.7K_+-1%

74AHC1G14: (schmitt trigger)
VCC=2.0~5.5V
Vi,max=7V
VT+,max=3.15V@Vcc=4.5V
VT-,min=1.35V@Vcc=4.5V
Voh,min=3.7V@Vcc=4.5V
Vol,max=0.55V@Vcc=4.5V

D-SUB+H/D_9_F15
VGA_COM0B
TP58 TP57 TP59 TP60
CM0_DCD CM0_DSR O_SER0_RX_CN O_SER0_RTS_L_CN O_SER0_TX_CN O_SER0_CTS_L_CN CM0_DTR CM0_RI

MUX_SER0_RX
R656 1K_+-1% 1/4W
R120602
CN_SER0_RX_R
Q8 NX7002AK_300mA/60V
CN_SER0_RX_1
U34 74AHC1G14_SOT23-5
C332 0.1uF_25V
CN_SER0_RX_2

74AHC1G14: (schmitt trigger)
VCC=2.0~5.5V
Vi,max=7V
VT+,max=3.15V@Vcc=4.5V
VT-,min=1.35V@Vcc=4.5V
Voh,min=3.7V@Vcc=4.5V
Vol,max=0.55V@Vcc=4.5V

UART MUX

1-2 BMC default
2-3 RS232
JP34 PH_3_2.54mm
P_+3V3SB
R2475 4.7K_+-1%
HW_UART0_SEL
0ohm_+-5% R2473
9 DB9_BMC_UART_SEL
0ohm_+-5% R2471
P_+3V3SB 4.7K_+-1% R2472 NI
X_10K_+-1% R2470
R2474 100K_+-1%
JP34_23 MINI-JUMP_2_S2.54mm

DB9
RS232

MUX_SER0_TX 2
MUX_SER0_RX 5
MUX_SER0_RTS_L 7
MUX_SER0_CTS_L 10

U68 TMUX1574RSVR_TI
0: A
1: B
VDD GND SEL EN
D1 D2 D3 D4
S1A S2A S3A S4A
S1B S2B S3B S4B
P_+3V3SB C2428 0.1uF_25V

CN_SER0_TX 5
CN_SER0_RX 5
CN_SER0_RTS_L 5
CN_SER0_CTS_L 5

BMC_UART_TX1_R 0ohm_+-5% R2932 BMC_HOST_UART_TX1 9
BMC_UART_RX1_R 0ohm_+-5% R2933 BMC_HOST_UART_RX1 9
BMC_HOST_UART_RTS1 9
BMC_HOST_UART_CTS1 9

Molude UART0
from SOC

BMC UART1(Console)

TMUX1574RSVR:
VCC=1.5~5.5V (Here is 1.8V)
Vih,min=1.2V
Vil,max=0.45V

5VCC_SB
C335 0.1uF_25V
U35
VCC GND
C1+ C1- C2+ C2- V- V+
C336 0.22uF_16V
C334 0.22uF_16V
C333 0.22uF_16V
C337 0.22uF_16V

TxIN:
Vih,min=2.4V
Vil,max=0.8V

SP3243E
-40~85

TxOUT:
Output Voltage Swing,min=+/-5V

CN_SER0_TX_2
CN_SER0_RTS_L_2
CN_SER0_RX_2
CN_SER0_CTS_L_2
T1IN T2IN T3IN R1OUT R2OUT R3OUT R4OUT R5OUT
T1OUT T2OUT T3OUT R1IN R2IN R3IN R4IN R5IN
O_SER0_TX_CN
O_SER0_RTS_L_CN
O_SER0_RX_CN
O_SER0_CTS_L_CN

RxOUT:
Voh,min=4.4V
Vol,max=0.4V

RxIN:
Range=-15V~15V
Input Threshold Low,min=0.8V
Input Threshold High,max=2.4V

5VCC_SB
SHUTDOWN
ONLINE
STATUS
R2OUT
0ohm_+-5% R4503
0ohm_+-5% R4502
SP3243EUEY-L_EXAR

VCC=5V
Icc,max=100mA
Data Rate=1000 kbps

5VCC_SB
P_+3V3SB
C338 0.1uF_25V
R661 4.7K_+-1%
CN_SER0_RTS_L_1
U36 74AHC1G14_SOT23-5
CN_SER0_RTS_L_2
MUX_SER0_RTS_L
Q9 NX7002AK_300mA/60V
R662 4.7K_+-1%

74AHC1G14: (schmitt trigger)
VCC=2.0~5.5V
Vi,max=7V
VT+,max=3.15V@Vcc=4.5V
VT-,min=1.35V@Vcc=4.5V
Voh,min=3.7V@Vcc=4.5V
Vol,max=0.55V@Vcc=4.5V

O_SER0_TX_CN C340 150pF_50V
O_SER0_RTS_L_CN C341 150pF_50V
O_SER0_RX_CN C342 150pF_50V
O_SER0_CTS_L_CN C343 150pF_50V

MUX_SER0_CTS_L
R663 1K_+-1% 1/4W
R120602
CN_SER0_CTS_L_R
Q10 NX7002AK_300mA/60V
CN_SER0_CTS_L_1
U37 74AHC1G14_SOT23-5
C339 0.1uF_25V
CN_SER0_CTS_L_2

74AHC1G14: (schmitt trigger)
VCC=2.0~5.5V
Vi,max=7V
VT+,max=3.15V@Vcc=4.5V
VT-,min=1.35V@Vcc=4.5V
Voh,min=3.7V@Vcc=4.5V
Vol,max=0.55V@Vcc=4.5V

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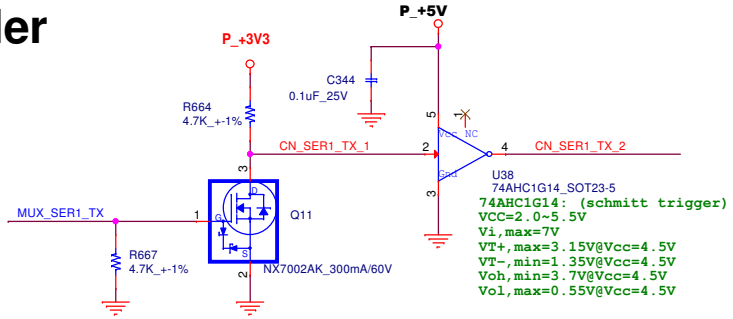
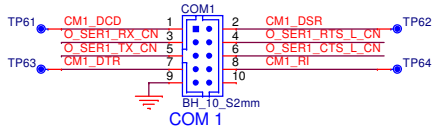
Title	UART0 COM1 from Module	
Size A3	Document Number COM-HPC Server Base	Rev A1
Date: Tuesday, April 11, 2023	Sheet 43 of 66	

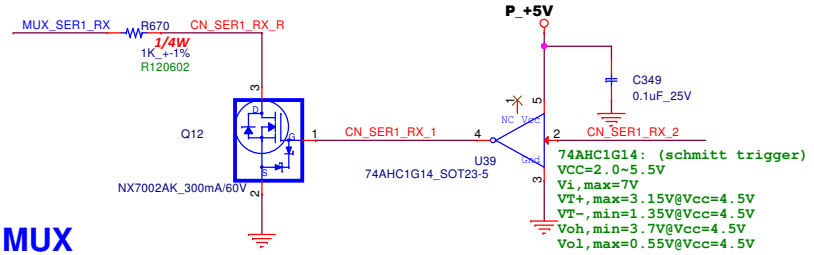
Molude UART1 with BOX header

Resever — Close to Q11 Q12

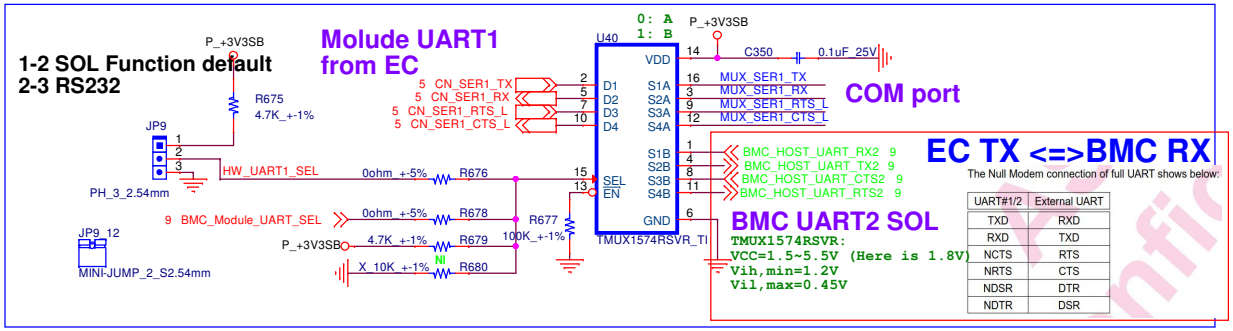
MUX_SER1_TX	R665	NI	0ohm +-1%	CN_SER1_TX_2
MUX_SER1_RX	R666	NI	0ohm +-1%	CN_SER1_RX_2
MUX_SER1_RTS_L	R668	NI	0ohm +-1%	CN_SER1_RTS_L_2
MUX_SER1_CTS_L	R669	NI	0ohm +-1%	CN_SER1_CTS_L_2

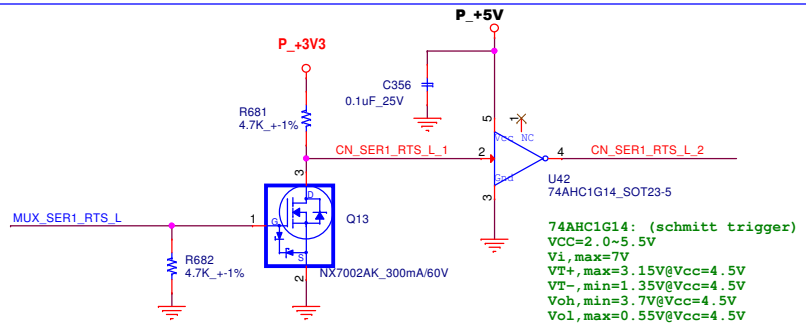


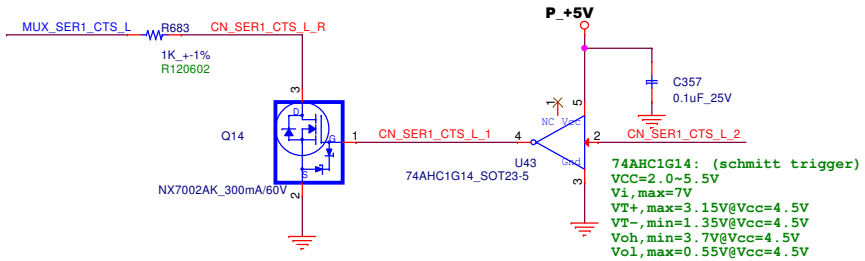


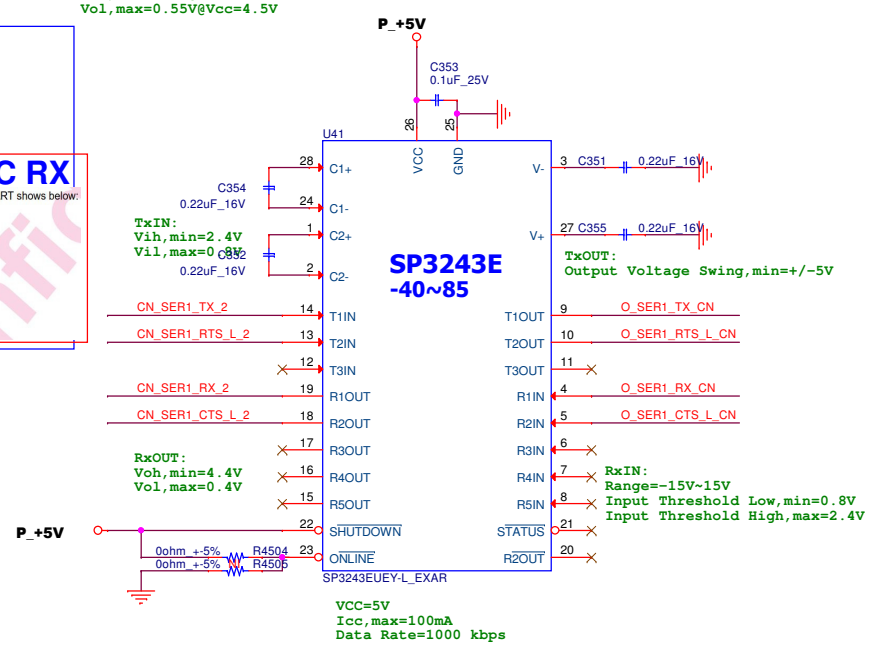


UART MUX









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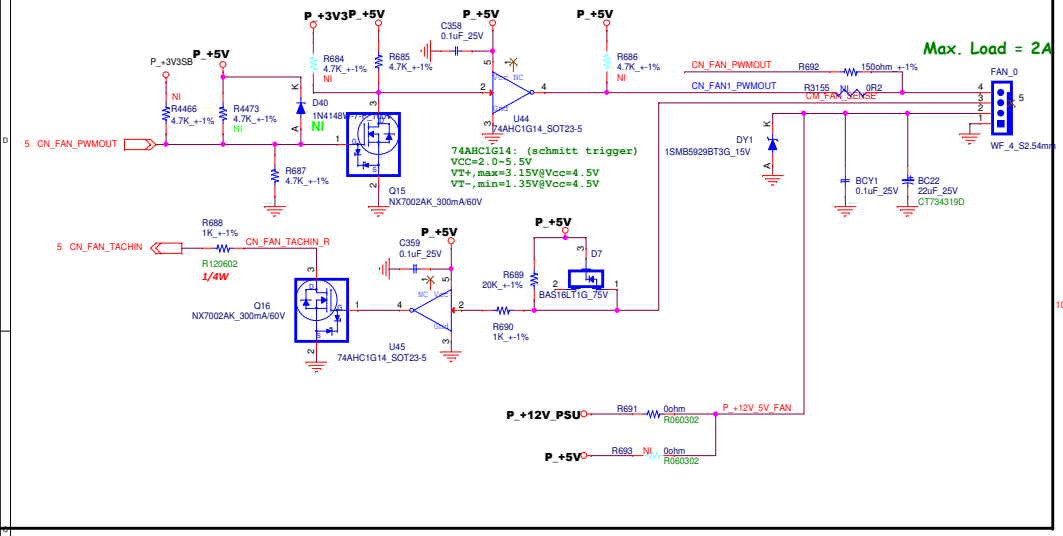
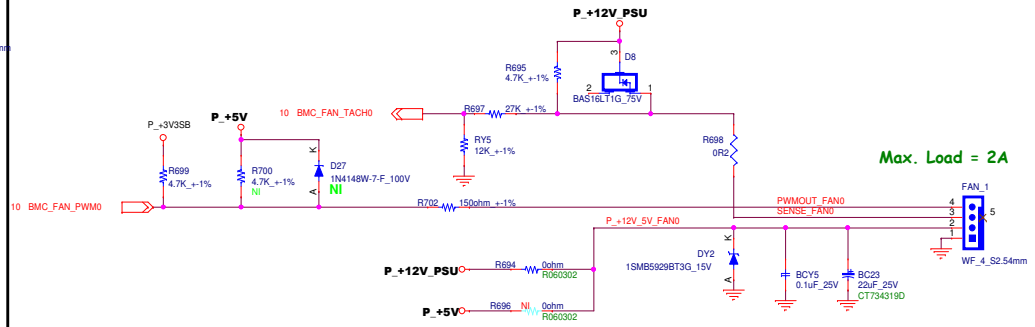
Title	UART1 COM2 from Module	
Size A3	Document Number COM-HPC Server Base	Rev A1
Date: Tuesday, April 11, 2023	Sheet 44 of 66	

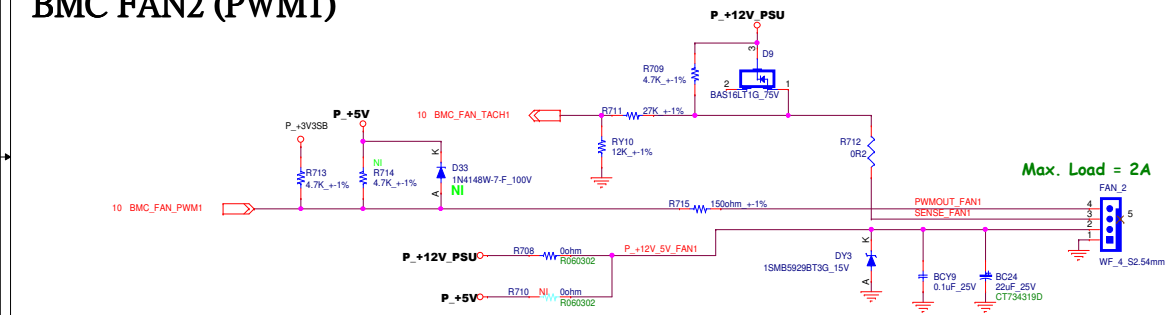
Module FAN0



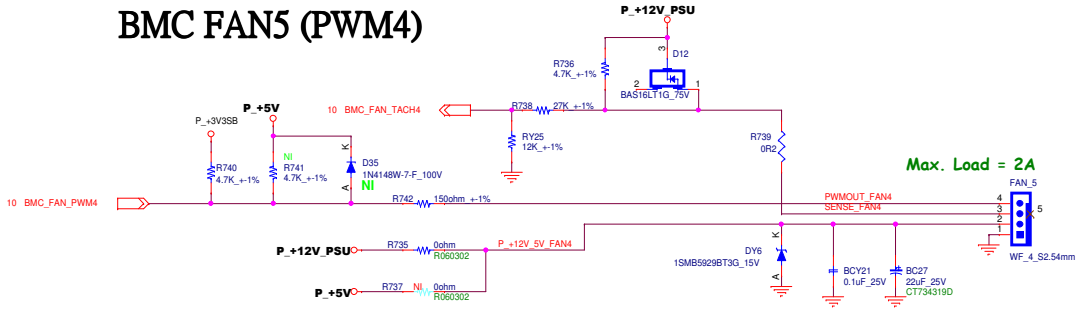
BMC FAN1 (PWM0)



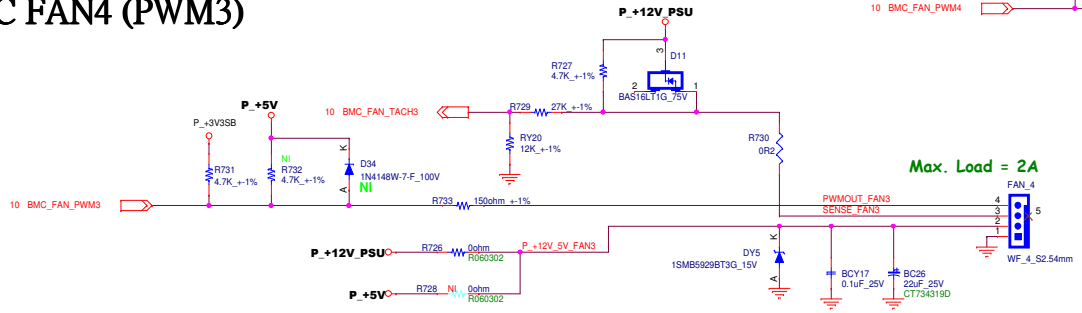
BMC FAN2 (PWM1)



BMC FAN5 (PWM4)



BMC FAN4 (PWM3)



<Variant Name>

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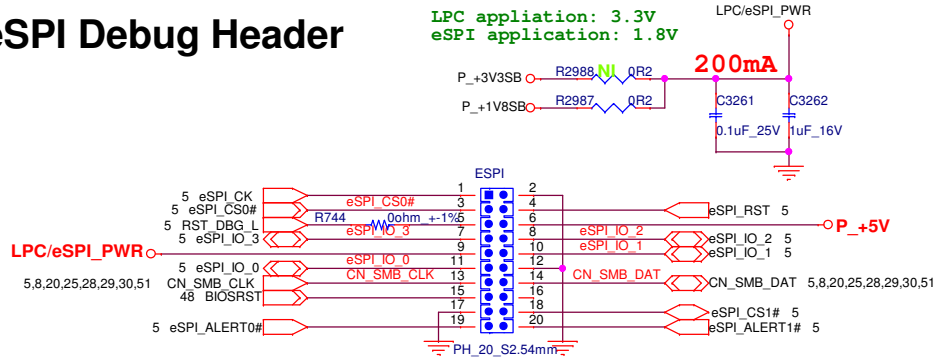
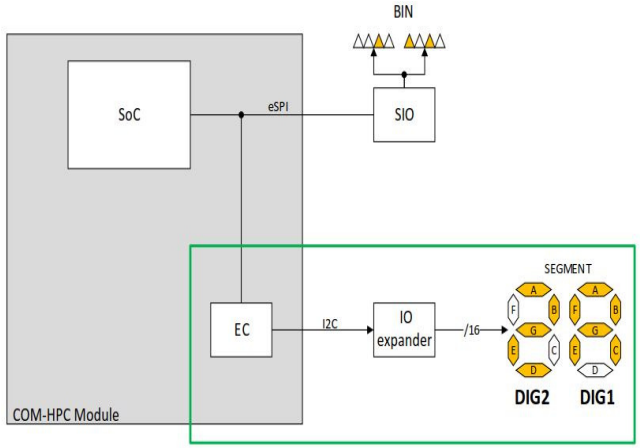
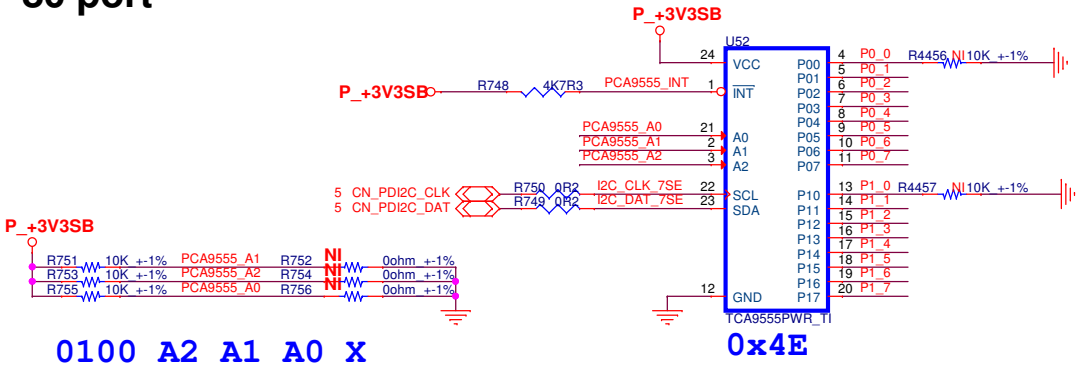
Title	Module FAN, BMC FAN	
Size C	Document Number COM-HPC Server Base	Rev A1
Date: Tuesday, April 11, 2023	Sheet 45 of 66	

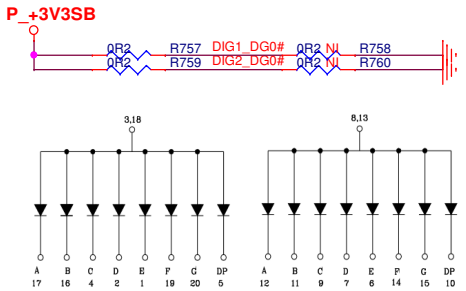
eSPI Debug Header





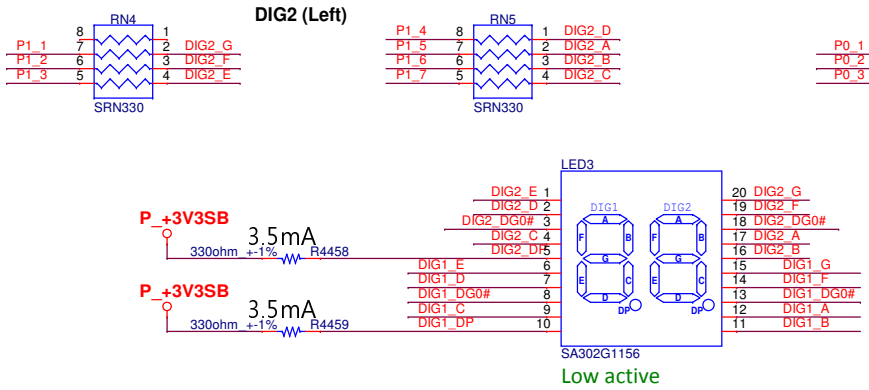
80 port

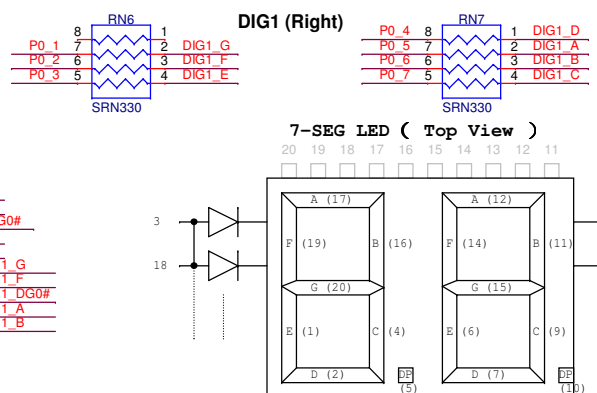




No	P7-C	P6-B	P5-A	P4-D	P3-E	P2-F	P1-G	P0	Hex
0	1	1	1	1	1	1	0	0	FC
1	1	1	0	0	0	0	0	0	C0
2	0	1	1	1	1	0	1	0	7A
3	1	1	1	1	0	0	1	0	F2
4	1	1	0	0	0	1	1	0	C6
5	1	0	1	1	0	1	1	0	B6
6	1	0	1	1	1	1	1	0	BE
7	1	1	1	1	0	0	0	0	E0
8	1	1	1	1	1	1	1	0	FE
9	1	1	1	1	0	1	1	0	F6
A	1	1	1	0	1	1	1	0	EE
B	1	0	0	1	1	1	1	0	9E
C	0	0	1	1	1	1	0	0	3C
D	1	1	0	1	1	0	1	0	DA
E	0	0	1	1	1	1	1	0	3E
F	0	0	1	0	1	1	1	0	2E
N0	P7-C	P6-B	P5-A	P4-D	P3-E	P2-F	P1-G	P0	Hex

<Variant Name>





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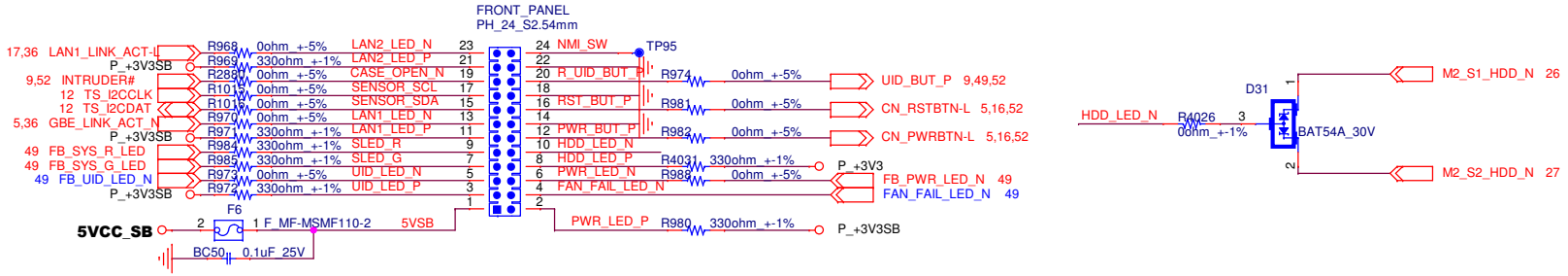
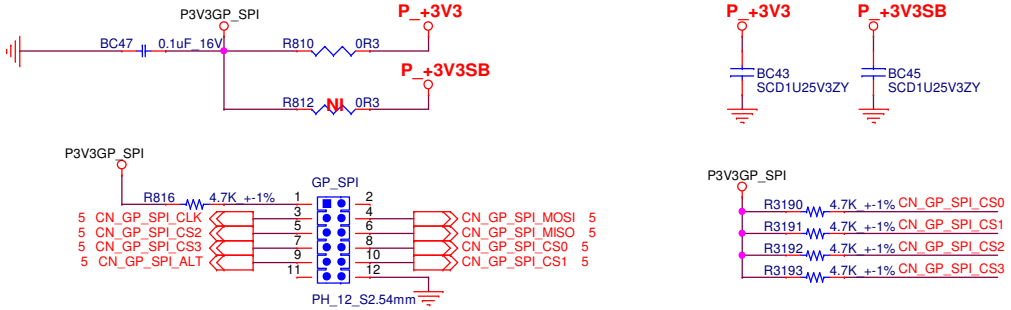
Title	Port80/eSPI CON	
Size B	Document Number COM-HPC Server Base	Rev A1
Date: Tuesday, April 11, 2023	Sheet 46 of 66	

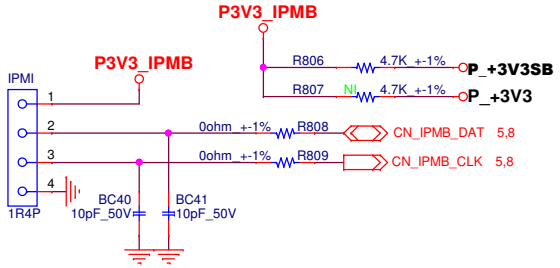
Follow with front panel board of Chenbro 2.54pitch cable side



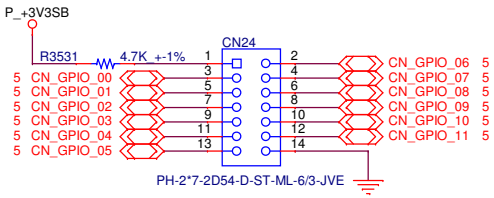
Module GPP_SPI Header



IPMB Header



Module GPIO Header



<Variant Name>

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Title	Front panel, Misc. Head	
Size B	Document Number COM-HPC Server Base	Rev A1
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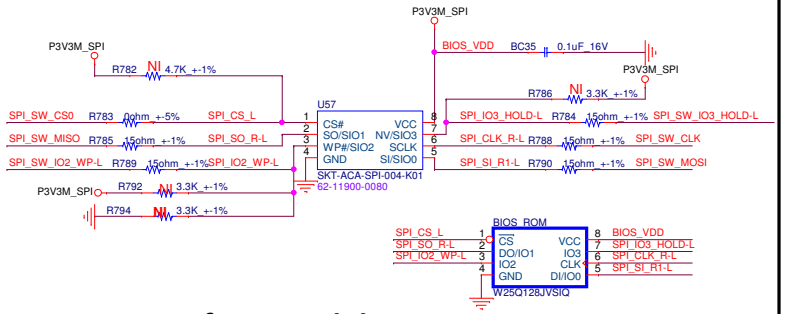
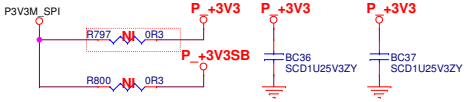
SPI BIOS ROM

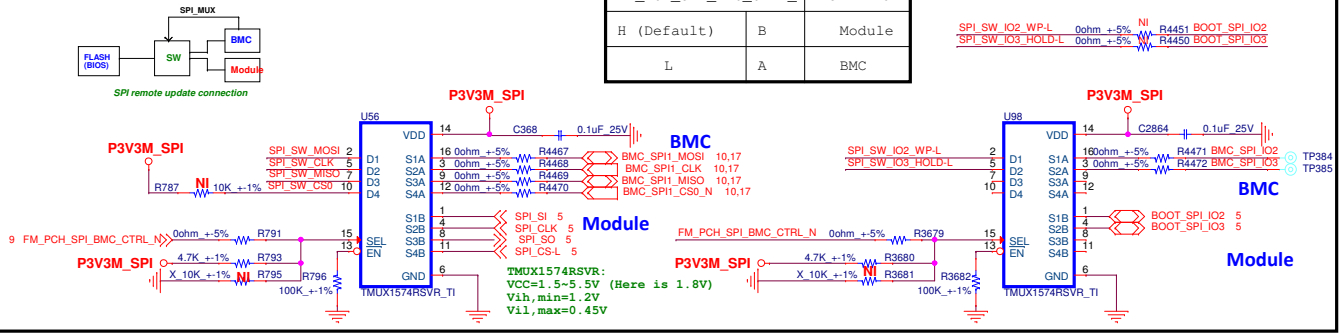


Power come from module



SPI select (High:Module, Low:BMC)

FM_PCH_SPI_BMC_CTRL_N		SPI From
H (Default)	B	Module
L	A	BMC



H1-2: / L:2-3

eSPI BIOS boot is not support, only support A and C

	JP29 SEL2	JP28 SEL1	JP27 SEL0	BIOS Boot Select (MAFS:SPI0 SPI1 / SAFS:eSPI0) Module	Carrier	Figure 7
(default)	1-2	1-2	1-2	SPI0 SPI1 eSPI0		A B
	1-2	1-2	2-3	SPI1 eSPI0	SPI0	A B C
	1-2	2-3	1-2	SPI0 eSPI0	SPI1	A B C
	1-2	2-3	2-3	Reserved for future use		
	2-3	1-2	1-2	SPI0 SPI1	eSPI0	A D
	2-3	1-2	2-3	SPI1	SPI0 eSPI0	A C D
	2-3	2-3	1-2	SPI0	SPI1 eSPI0	A C D
	2-3	2-3	2-3		eSPI0	D

The signals should be pulled up on Module to vendor specific power rail

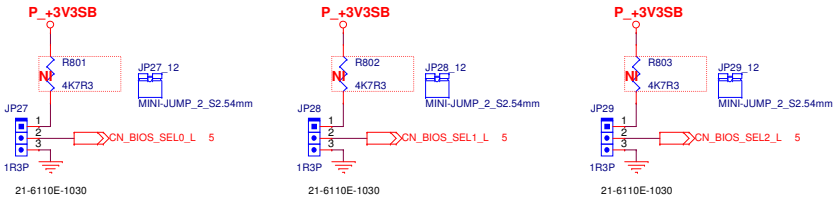
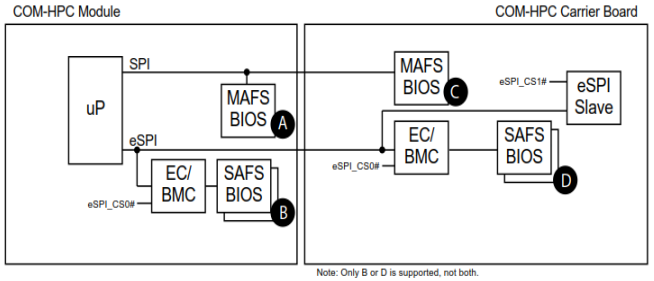
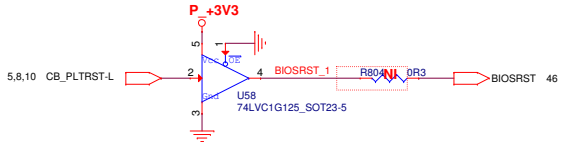


Figure 7: MAFS and SAFS BIOS Configurations





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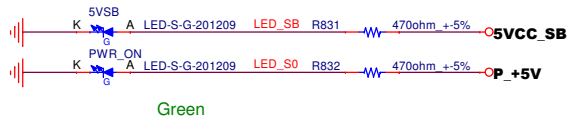
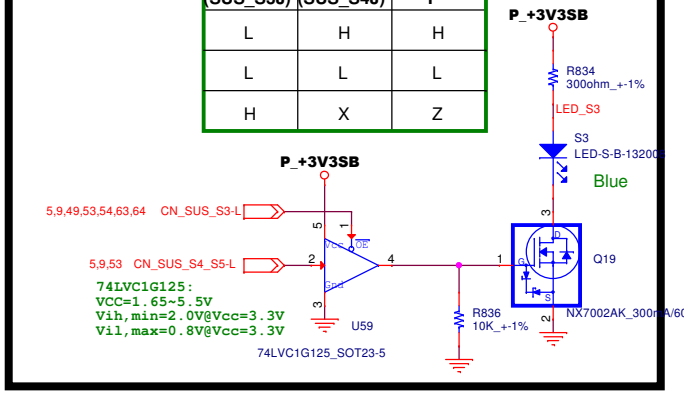
Title	BIOS Boot Select & SPI ROM	
Size: Custom	Document Number: COM-HPC Server Base	Rev: A1
Date: Tuesday, April 11, 2023	Sheet 48 of 66	

Power LED

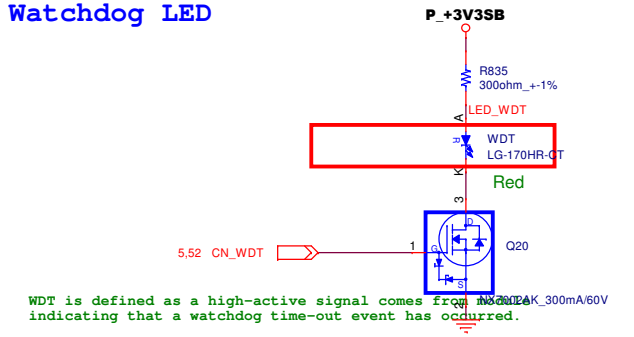


S3 LED

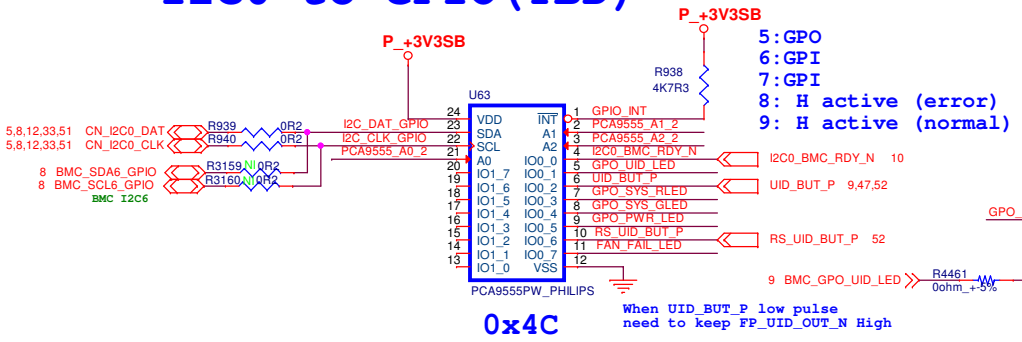
OE# (SUS_S3J)	A (SUS_S4J)	Output Y
L	H	H
L	L	L
H	X	Z



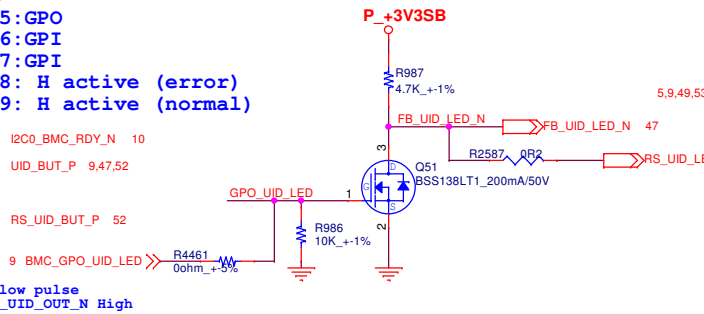
Watchdog LED



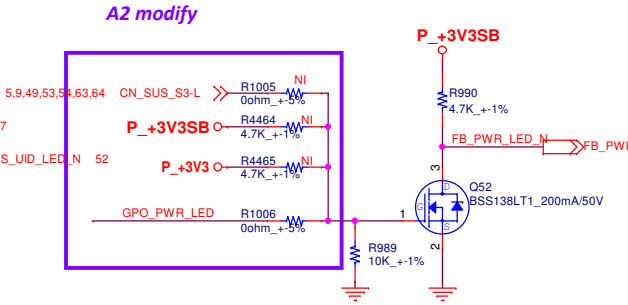
I2C0 to GPIO(TBD)

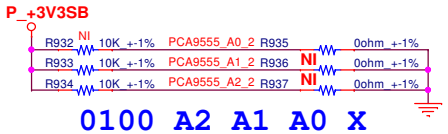


UID LED

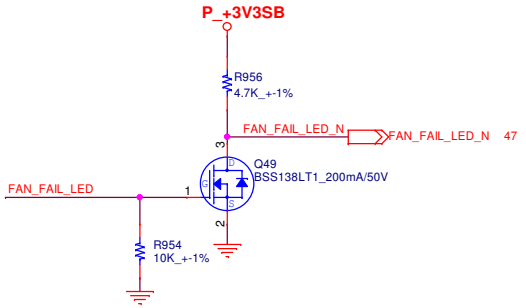


PWR LED



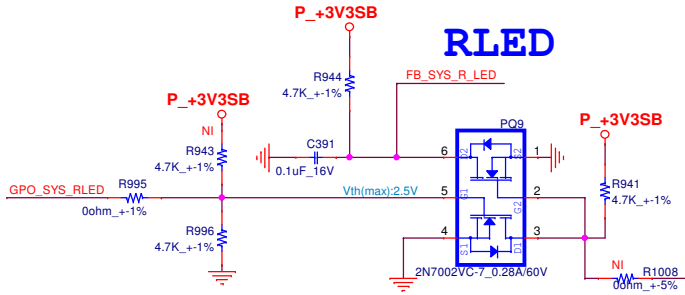


FAN Fail LED

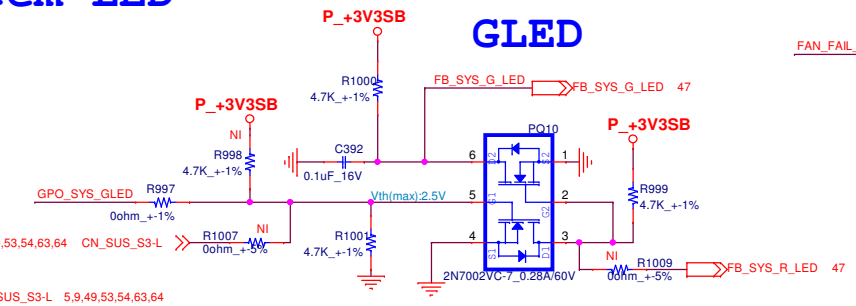


System LED

RLED



GLED



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Title	LEDs, I2C0 to GPIO	
Size A3	Document Number COM-HPC Server Base	Rev A1
Date: Tuesday, April 11, 2023	Sheet 49 of 66	

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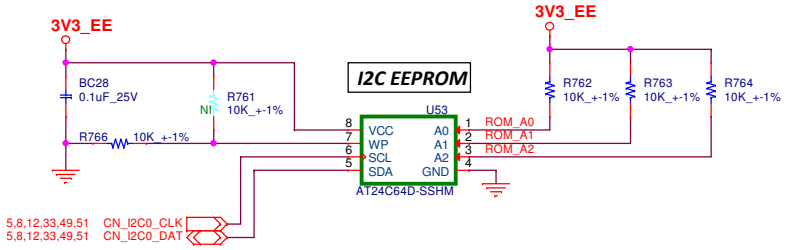
Title

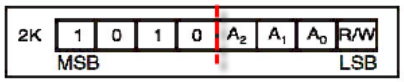
Size	Document Number	Rev
A3	COM-HPC Server Base	A1

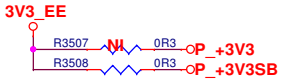
Date:	Tuesday, April 11, 2023	Sheet	50	of	66

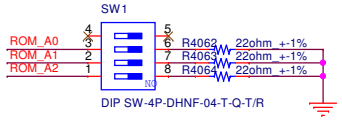
COM-HPC Carrier Board EEPROM

sing the Unique Device Id and describes
the expected PCI Express link configuration





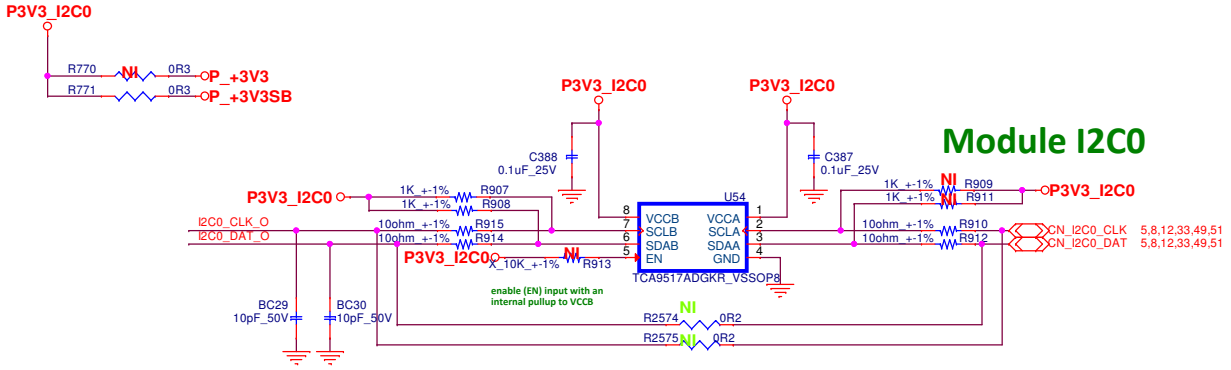




SW1 I2C EEPROM_U53	
1-8	A2_OFF (High)
2-7	A1_OFF (High)
3-6	A0_OFF (High)

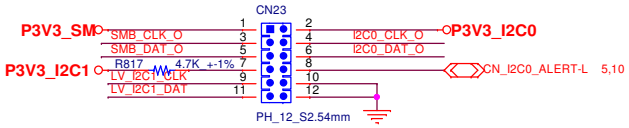
Default Address:AEh

I2C0 Buffer to External Header



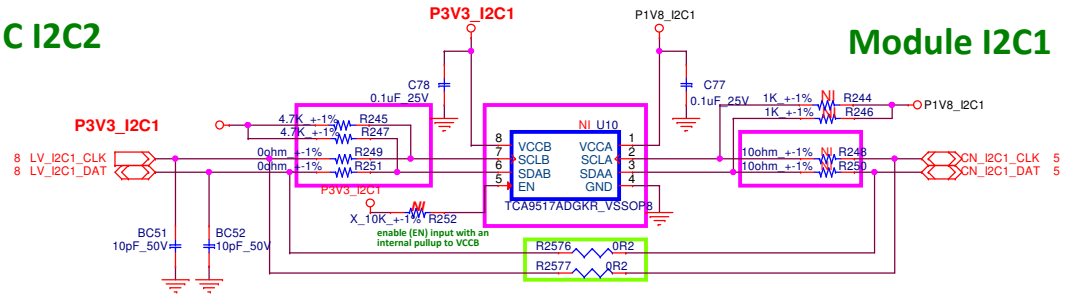
I2C1 Buffer to External Header

Module I2C0/1 and SMB external header

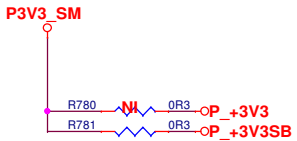


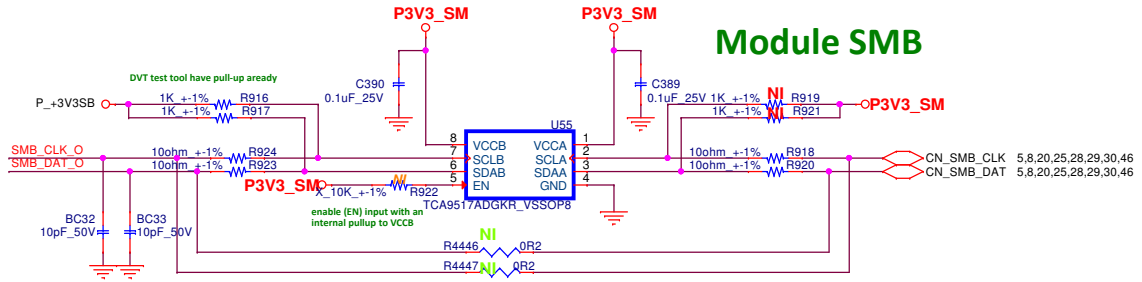
BMC I2C2

Module I2C1



SMBus Buffer to External Header





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Title	SMBus, I2C0, I2C1, EEPROM	
Size A3	Document Number COM-HPC Server Base	Rev A1
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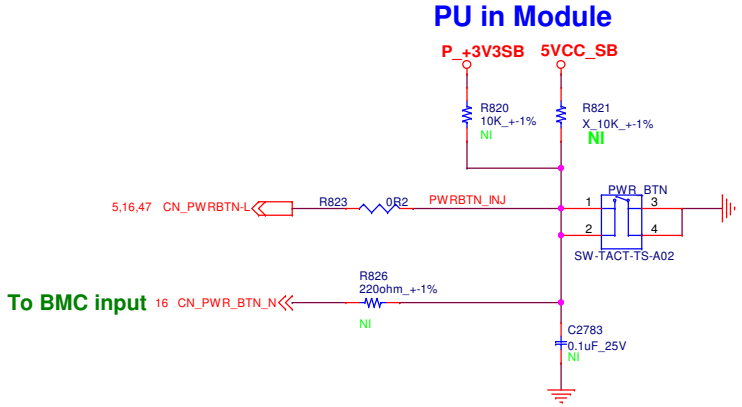
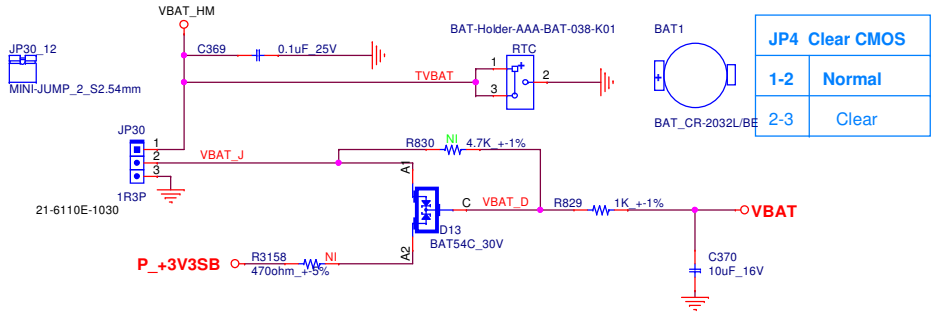
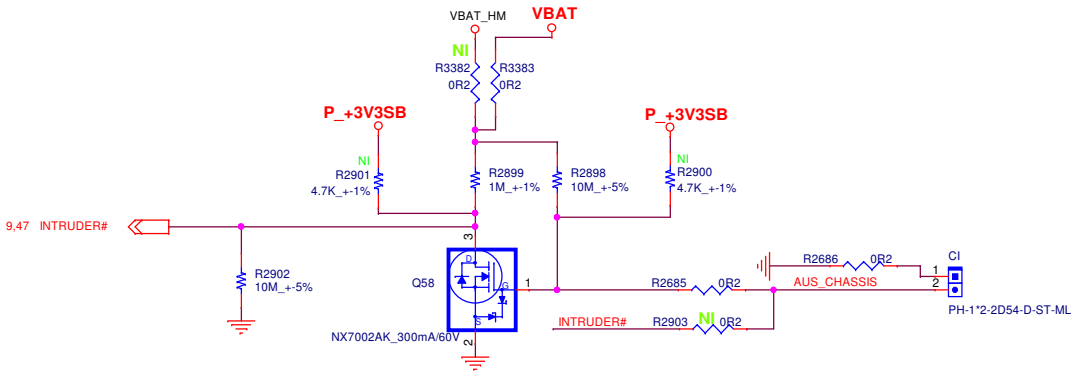
PWR BTN



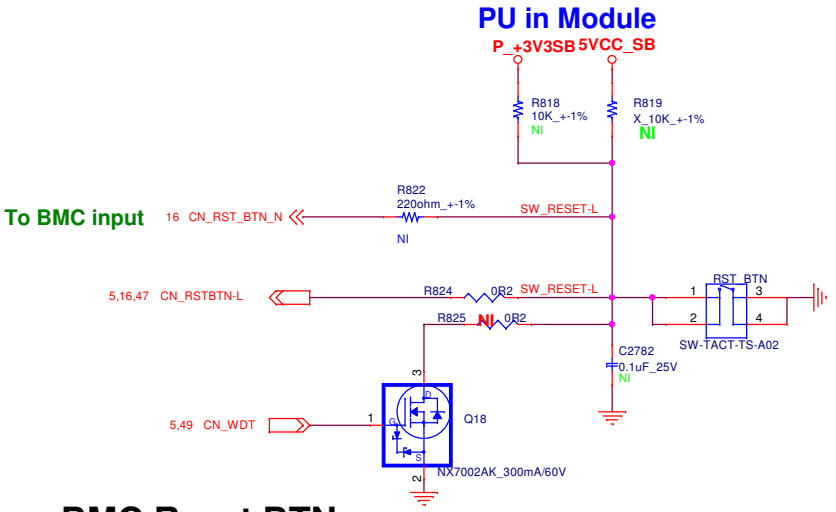
RTC BATT.



CHASSIS INTRUSION

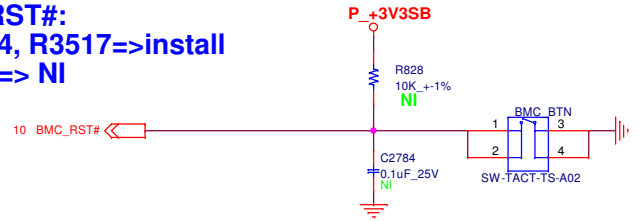


Reset BTN

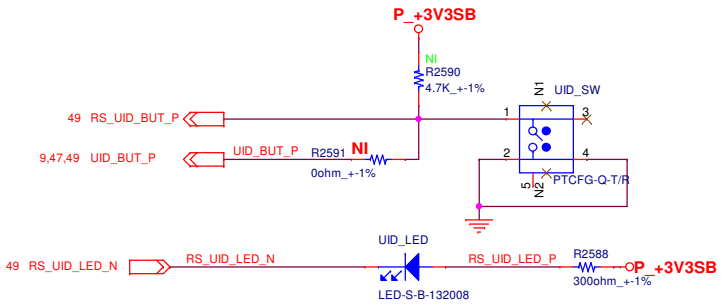


BMC Reset BTN

SRST#:Default
EXTRST#:
C2784, R3517=>install
R166=> NI



UID LED for rear side



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Title	Switch Buttons / RTC Battery	
Size A3	Document Number COM-HPC Server Base	Rev A1
Date: Tuesday, April 11, 2023	Sheet 52 of 66	

Dummy Loads

P_+3V3_ATX

Trace Width 40mils

NI R858 3ohm_+-1% R251203

P_+3V3_ATX_R

NI R860 3ohm_+-1% R251203

Pd=(3.3/6)^2*3=0.9W

P_+5V_ATX

NI R862 3ohm_+-1% R251203

P_+5V_ATX_R1

NI R863 3ohm_+-1% R251203

P_+5V_ATX_R2

NI R864 3ohm_+-1% R251203

Pd=(5/9)^2*3=0.93W

ATX Power Min. Current:
1. +12V1, +12V2: 1A
2. +5V: 0.3A
3. +3.3V: 0.5A
4. -12V: 0A
5. +5VSB: 0A

ATX 24Pin Connector

ATX_24 POWER_24_S4.2mm

P_+3V3_ATX, P_+5V_ATX, P_-12V_ATX, PSU_PSON-L, P_+5V_SB_PSU, PSU_PWR_OK, P_-5V_ATX, P_+5V_ATX, P_+5V_SB_PSU, P_+12V_PSU, P_+3V3_ATX

PS_ON#
Vih,min=2.0V
Vil,max=0.8V
The power supply shall provide an internal pull-up to TTL high.

5VCC_SB, P_+5V, R2578 4.7K_+-1%, R2579 4.7K_+-1%, R2580 10K_+-1% NI, Q54 NX7002AK_300mA/60V

P_+3V3, P_+3V3SB, R861 4.7K_+-1%, R2581 4.7K_+-1% NI, Q55 NX7002AK_300mA/60V, R4492 0ohm_+-1% NI, 64 P_+1V8_PG

P_+3V3SB, C371 0.1uF_25V, CB_PWROK, U60 74LVC1G125_SOT23-5
74LVC1G125:
VCC=1.65~5.5V
Vih,min=2.0V@Vcc=3.3V
Vil,max=0.8V@Vcc=3.3V
R859 0ohm_+-1% NI, CN_VIN_PWR_OK

PU in Module

CN_VIN_PWR_OK 5

P_+3V3_ATX: C373 0.1uF_25V
P_+5V_ATX: C374 0.1uF_25V
P_-12V_ATX: C375 0.1uF_25V
P_+12V_PSU: C376 0.1uF_25V
P_-5V_ATX: C377 0.1uF_25V
P_+5V_SB_PSU: C378 0.1uF_25V

Close to CN25

A2 modify

3A 120mil ATX PSU

P_+5V_SB_PSU, JP35 PH-1*4-2D54-D-ST-ML, R1909 0.0005ohm_+-1%, JP35_23 MINI-JUMP_2_S2.54mm, C2870 10uF_10V C060304, VCC_5V_SBY_IN

3A 120mil DC to DC

P_+5VSB, R3692 0.0005ohm_+-1%

ATX 8Pin Connector

AON6407: P-Channel
Vds,max=-30V,Vgs,max=+/-25V
Id,max=-85A
Vgs(th)=-1.6~-2.6V
Rds(on,max)=6m-ohm@Vgs=-6V,Id=-20A

P_+12V_PSU, C379 0.1uF_25V, TC17 22uF_25V CT734319D, TC18 22uF_25V CT734319D, ATX_8 POWER_8_S4.2mm, C380 0.1uF_25V

QY7 AON6407_-85A/-30V, QY8 AON6407_-85A/-30V

To COMe Module P12V_MOD

EN_P_+12V_MOD-L_R, P_+12V_MOD_SS, R877 100ohm_+-1%, C382 0.01uF_50V

P_+12V_PSU, R873 10K_+-1%, R874 15K_+-1%

2N7002VC:
Id=280mA, Vgss=+/-20V
Vgs(th)=1.0~2.5V,
Rds(on)=7.5ohm

Q44 2N7002VC-7_0.28A/60V, R879 10K_+-1%, EN_P_+12V_MOD-L, R880 10K_+-1%, P_+12V_PSU

5VCC_SB, P_+5VSB, R868 NI 4K7R3, 5,62 CN_TYPE0-L, R869 NI 0ohm_+-1%, R870 0ohm_+-1%

C381 0.1uF_25V, R871 10K_+-1%, R872 10K_+-1% NI, O_PSON-L_R, R876 0ohm_+-1%, U62 74LVC1G125_SOT23-5

PSU_PSON-L 63, 5V, PSON_OUT-L, PSU_PSON-L

SUS3_5J, Q43 NX7002AK_300mA/60V

5,9,49,54,63,64 CN_SUS_S3-L, R878 1K_+-1%, S3J, JP32

5,9,49 CN_SUS_S4_S5-L, R881 1K_+-1%, S5J

PH_3_2.54mm

JP32_12 MINI-JUMP_2_S2.54mm

R882 0ohm_+-1%, PSON_OUT2-L, CEX_12V_EN-L, 62 CEX_12V_EN-L

R3359 NI 0ohm_+-1%, P12V_MOD_EN

62 MODULE_12V_ON_OFF_L, R3360 0ohm_+-1%

JP2 Power buttom active	
1-2	SUS_S3# (Default)
2-3	SUS_S5#

JP31 JP31_12 MINI-JUMP_2_S2.54mm PH_3_2.54mm

Power Supply

1-2	ATX
2-3	AT

(default)

JP33 JP33_12 MINI-JUMP_2_S2.54mm PH_3_2.54mm

COMe Module VCC_12V on off during S3/S5

1-2	12V off during S3 /S5
2-3	12V on during S3/S5

(default)

4 Power Mode

	Power Supply	C-HPC Module	JP31	JP33	JP35	12V POWER
	Jumper Setting					
(default)	ATX	ATX	1-2	1-2	2-3	OFF
	AT	AT	2-3	2-3	X	ON
	AT	ATX	2-3	1-2	X	OFF

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Title	ATX Power & 2 Modes	
Size A3	Document Number COM-HPC Server Base	Rev A1
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P_+5V/P_+3V3(TPS51220)

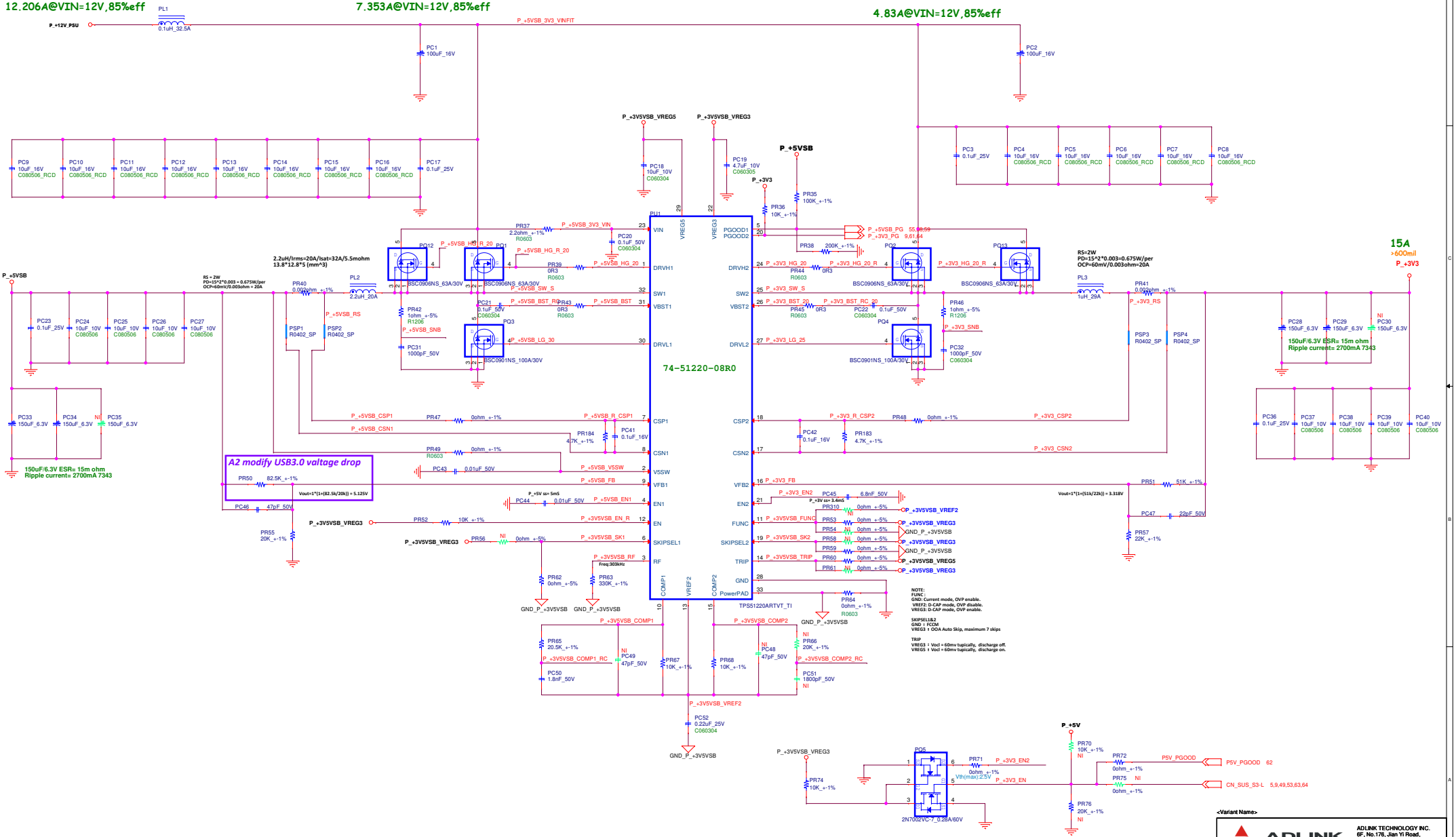
P_+5V VR Specification:	P_+3V3 VR Specification:
Vout: 5.0V Imax: 15A Istep: 4.5A Slew Rate: 1A/uS TOB: + - 5.0% Switching Frequency per Phase: 303kHZ	Vout: 3.3V Imax: 15A Istep: 12A Slew Rate: 1A/uS TOB: + - 5.0% Switching Frequency per Phase: 303kHZ

TPS51220. power sequence
1. VIN
2. PIN22 VREG3(Internal LDO)
3. PN29 VREG5(Internal LDO)
4. EN
5 Output
6. PGOOD

12V
12.206A@VIN=12V,85%eff

12V
7.353A@VIN=12V,85%eff

12V
4.83A@VIN=12V,85%eff



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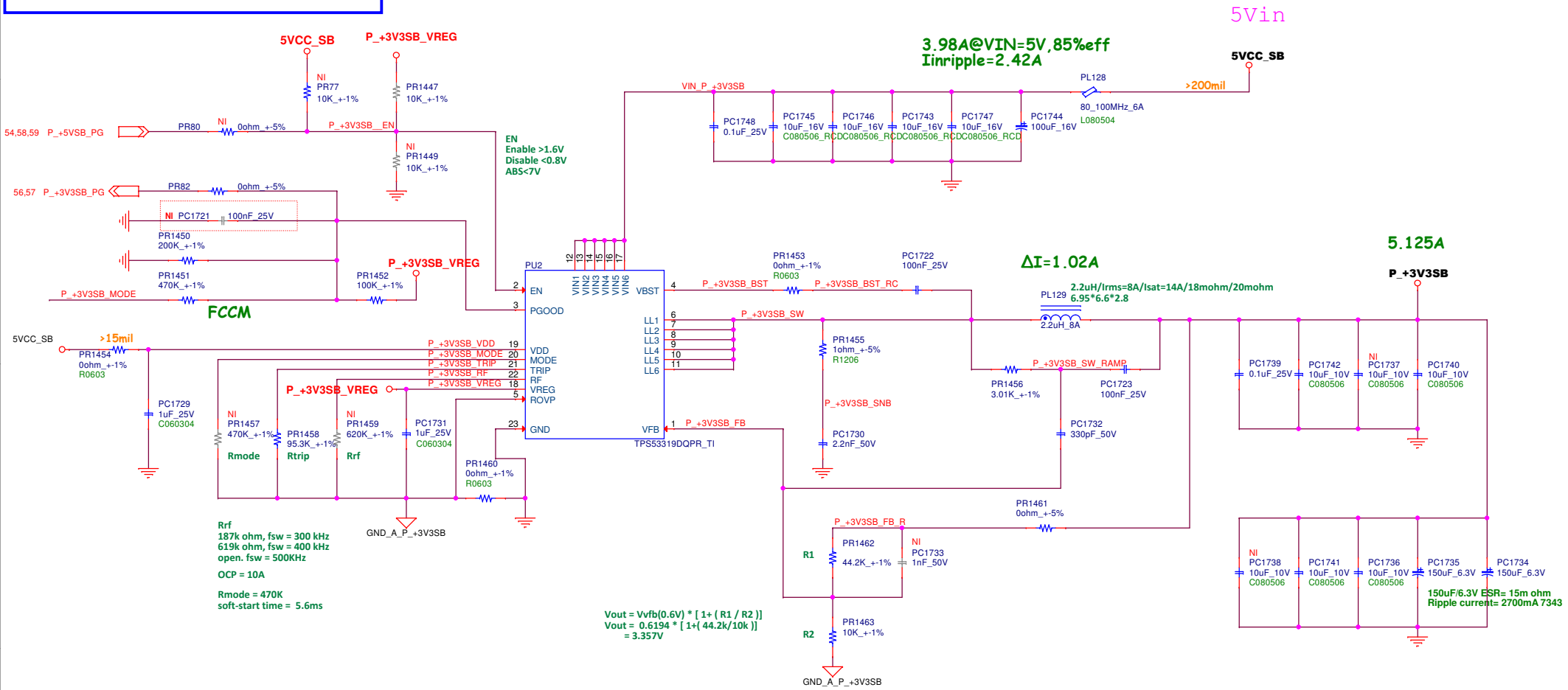
Title		
P_+3V3/P_+5VSB(TPS51220)		
Size: A2	Document Number: COM-HPC Server Base	Rev: A1
Date: Tuesday, April 11, 2023	Sheet 54 of 66	

P_+3V3SB(TPS53319)

P_+3V3SB Specification:
Vout: 3.3V
Imax: 5.125A
Istep: 3A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 500kHZ

TPS53319 power sequence
1. PIN19 VDD
2. PIN18 VREG internal 5V
3. VIN
4. PIN2 EN
5. Output
6. PIN3 PG



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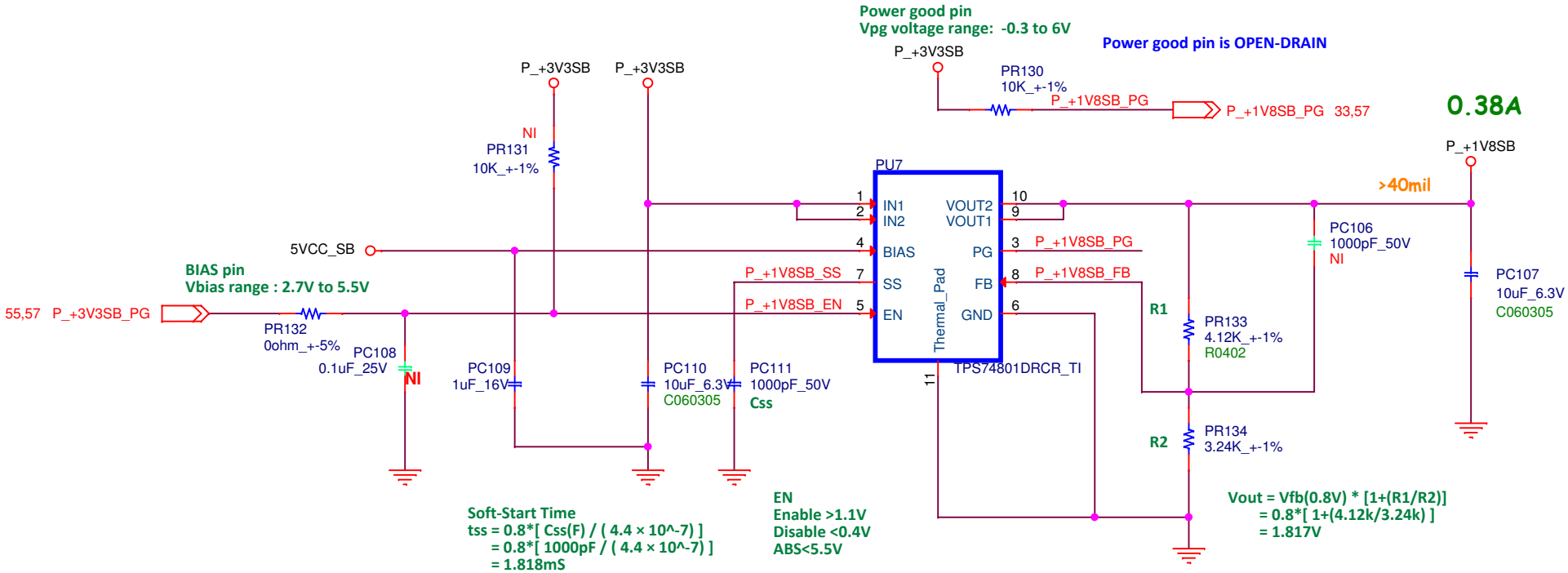
Title	P_+3V3SB(TPS53319)	
Size A3	Document Number COM-HPC Server Carrier	Rev A1
Date: Tuesday, April 11, 2023	Sheet 55 of 66	

P_+1V8SB(TPS74801)

P_+1V8SB Specification:
Vout: 1.8V
Imax: 0.38A
Istep: 0.25A
Slew Rate: 1A/uS
TOB: + - 5.0%

TPS74801 power sequence
1. PIN4 BIAS
2. VIN
3. EN
4. Vout
5. PG



(3.3-1.8)*0.5*42+85=116.137degC

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Title	P_+1V8SB(TPS74801)	
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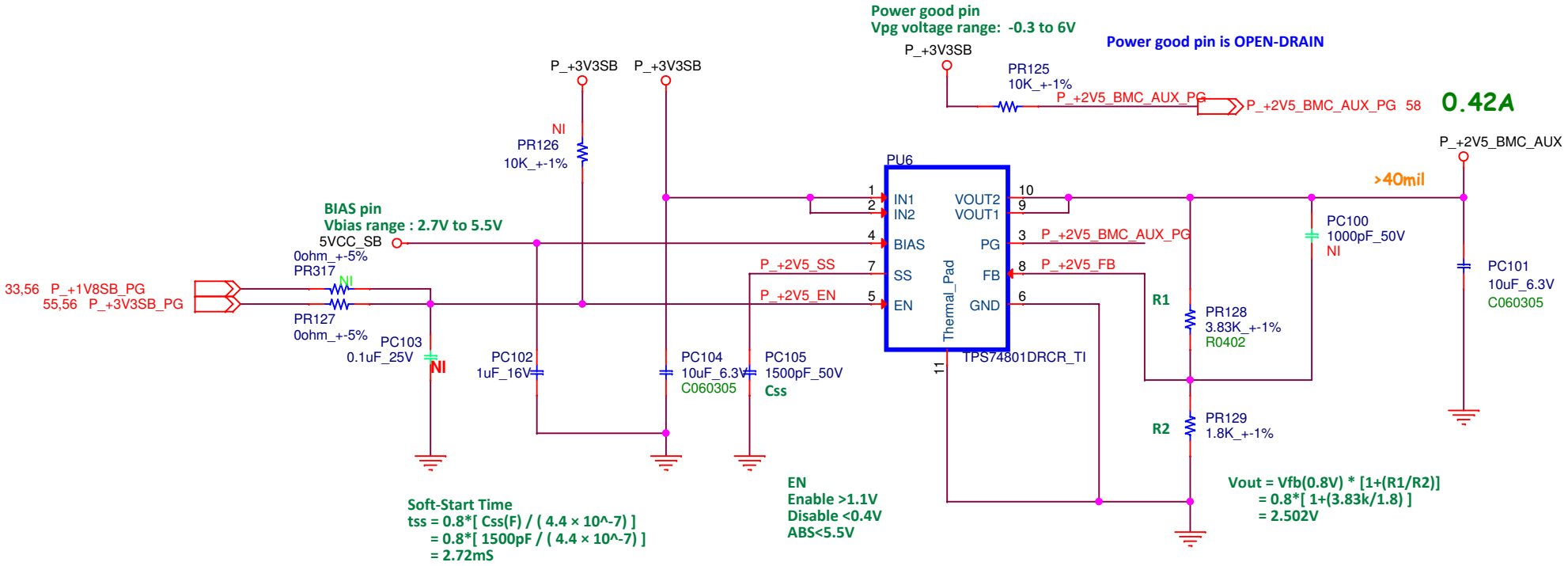
P_+2V5_BMC_AUX(TPS74801)

P_+2V5_BMC_AUX Specification:
Vout: 2.5V
Imax: 0.42A
Istep: 0.25A
Slew Rate: 1A/uS
TOB: + - 5.0%

TPS74801 power sequence
1. PIN4 BIAS
2. VIN
3. EN
4. Vout
5. PG



(3.3-2.5)*0.5*42+85=101.75degC

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Title	P_+2V5_BMC_AUX(TPS74801)	
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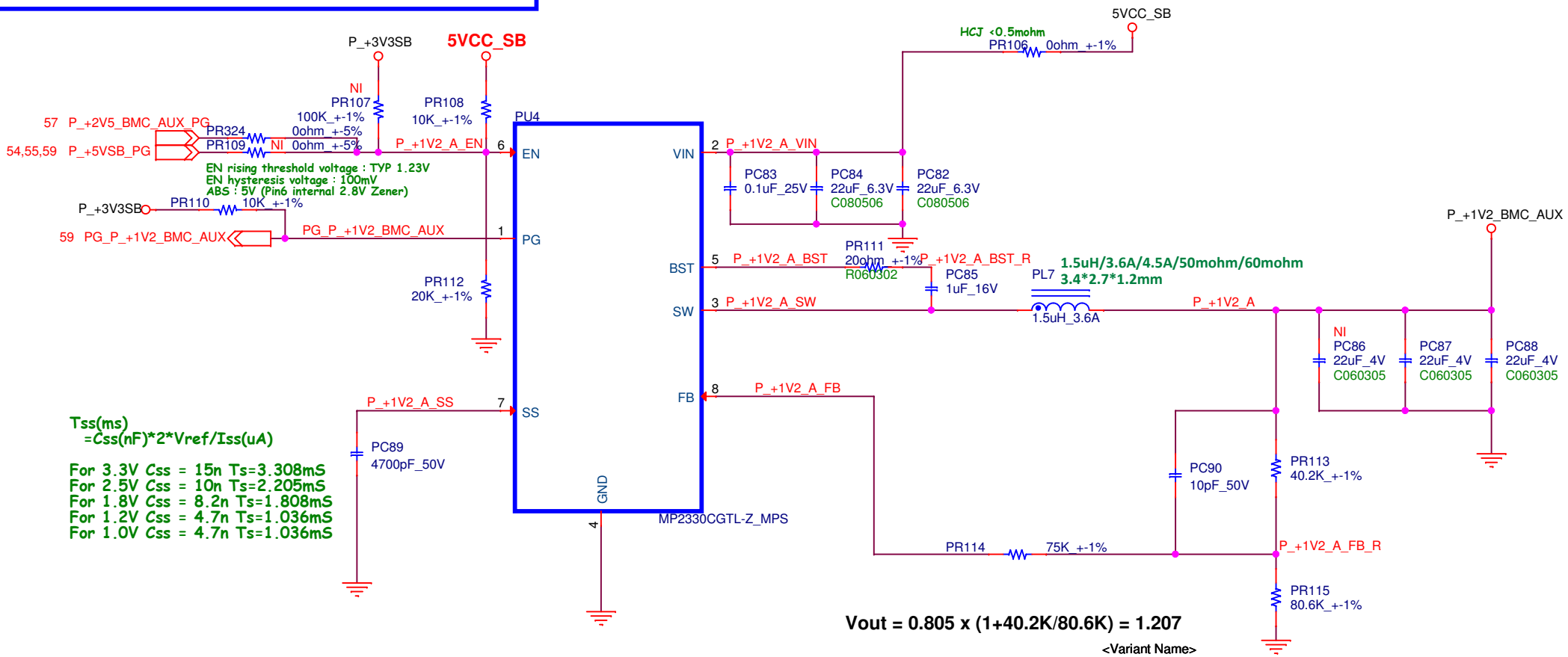
P_+1V2_BMC_AUX(MP2330C)

P_+1V2_BMC_AUX Specification:
Vout: 1.2V
Imax: 1.1A
Istep: 0.6A
Slew Rate: 2.5A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 650kHZ

MP2330C power sequence
1. VIN
2. PIN6 EN
3. Output
4. PIN1 PG

12V
0.3123A@VIN=5V,85%eff



Tss(ms)
=Css(nF)*2*Vref/Iss(uA)

For 3.3V Css = 15n Ts=3.308mS
For 2.5V Css = 10n Ts=2.205mS
For 1.8V Css = 8.2n Ts=1.808mS
For 1.2V Css = 4.7n Ts=1.036mS
For 1.0V Css = 4.7n Ts=1.036mS

Vout = 0.805 x (1+40.2K/80.6K) = 1.207

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Title	P_+1V2_BMC_AUX(MP2330C)	
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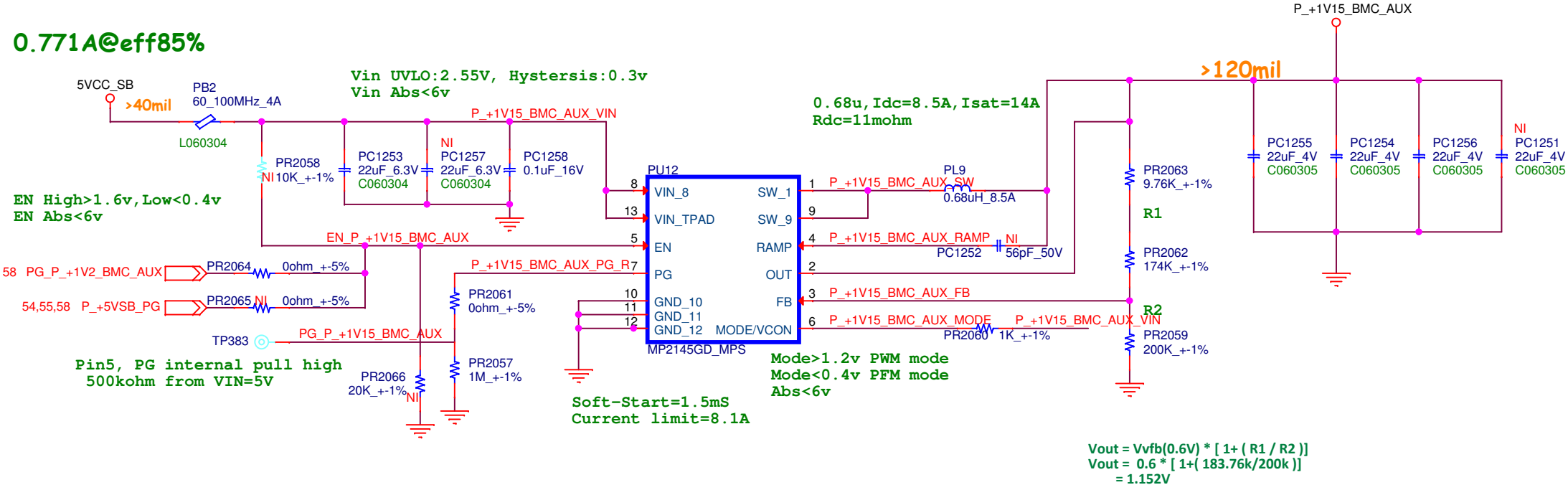
P_+1V15_BMC_AUX(MP2145)

P_+1V0_A Specification:
Vout: 1.15V
Imax: 2.85A
Istep: 1.425A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 1.2MHZ
operation tempeture : 85 degree

MP2145 power sequence
1. VIN
2. EN
3. Output

1.15*2.85*((1/0.87)-1)*70+85=119.28degC

0.771A@eff85%



Vout = Vvfb(0.6V) * [1+ (R1 / R2)]
Vout = 0.6 * [1+(183.76k/200k)]
= 1.152V

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Title	P_+1V15_BMC_AUX(MP2145)	
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Title

P_+1V15SB(TPS82085)

Size	Document Number	Rev
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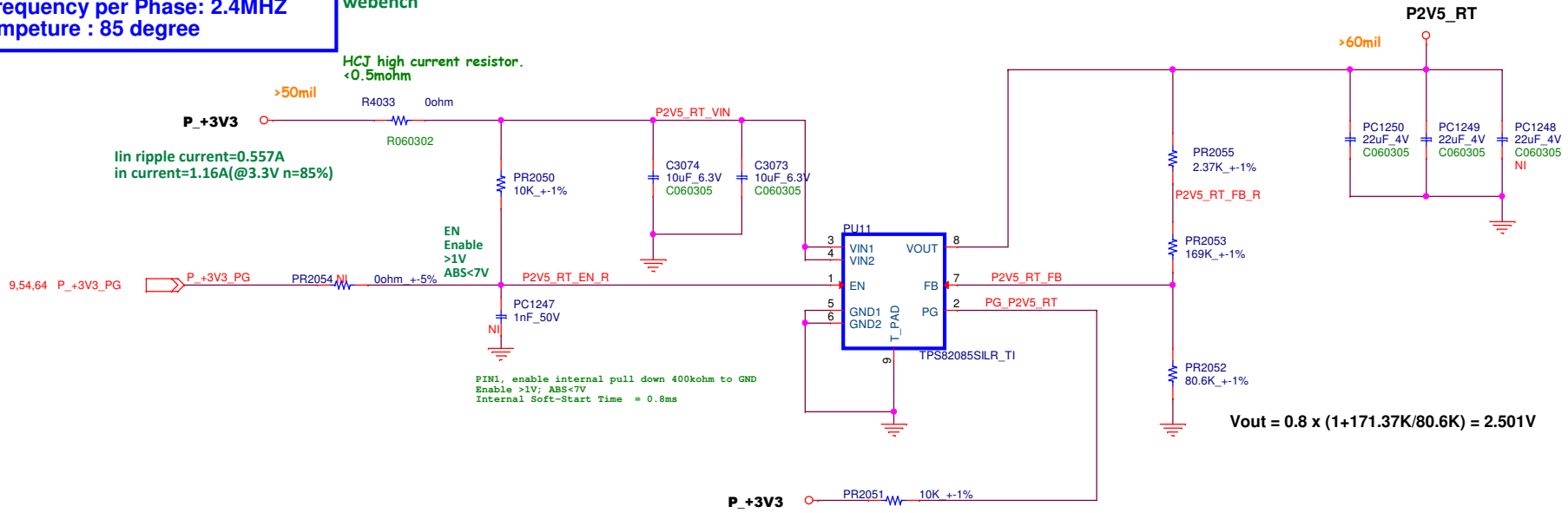
P2V5_RT (TPS82085)

P2V5_RT Specification:
Vout: 2.5V
Imax: 1.3A
Istep: 0.65A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 2.4MHZ
operation tempeture : 85 degree

TPS82085 power sequence
1. VIN
2. EN
3. Output

0.18261*64.6+85=96.79degC
webench

1.3A



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Title	P2V5_RT(TPS82085)	
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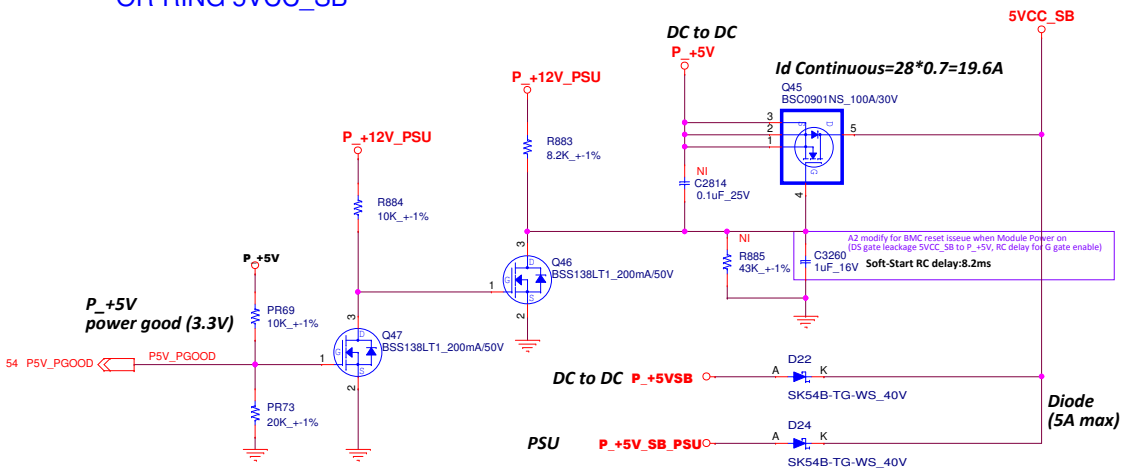
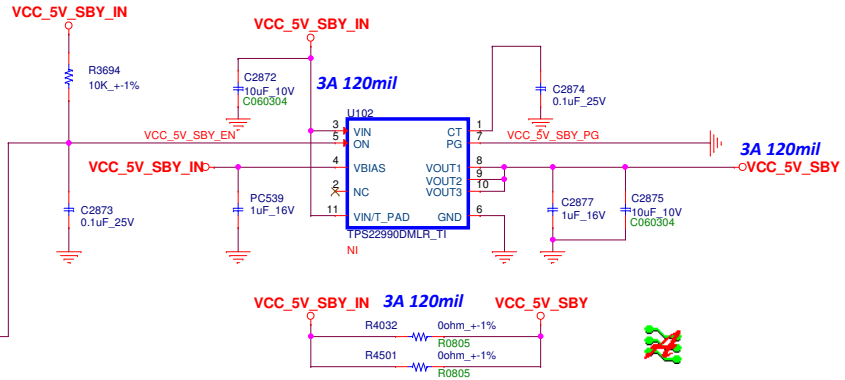
OR-RING 5VCC_SB



	Module Connections			Meaning
Ref	TYPE2	TYPE1	TYPE0	
7	NC	NC	NC	Reserved
6	NC	NC	GND	Reserved
5	NC	GND	NC	Reserved
4	NC	GND	GND	Server Module – Fixed 12V input
3	GND	NC	NC	Reserved
2	GND	NC	GND	Reserved
1	GND	GND	NC	Client Module - Wide Range 8V to 20V input
0	GND	GND	GND	Client Module – Fixed 12V input

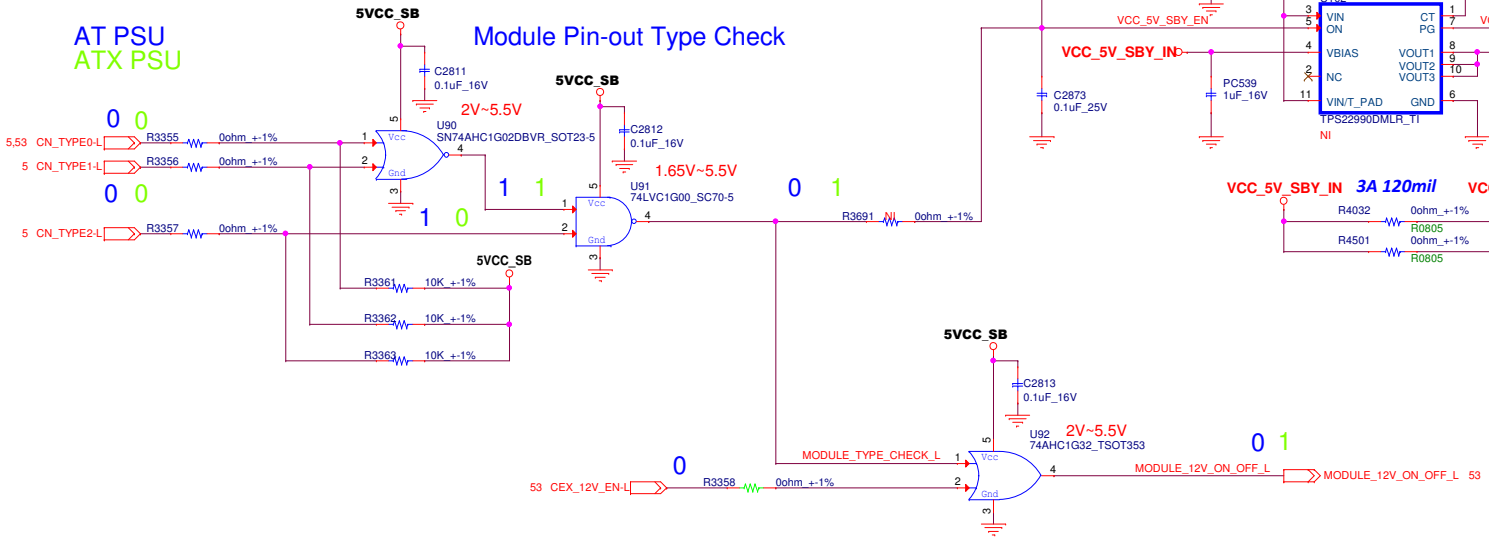
Module VCC_5V_SBY Power Switch / 2A

TPS22990
Vin= 0.6-5.5V, VBAIS=2.5-5.5V
Rds(on)= 3.9m ohm, Vin=5.0V, VBIAS=5.0V
Rds(on)= 3.9m ohm, Vin=3.3V, VBIAS=3.3V
Imax=10A



AT PSU
ATX PSU

Module Pin-out Type Check



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Title: 5VCC_SB & Module type check

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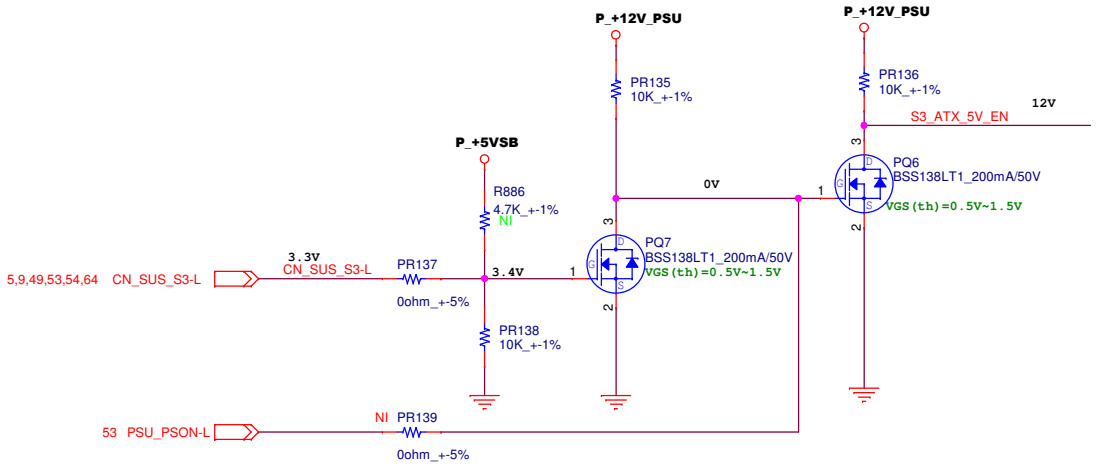
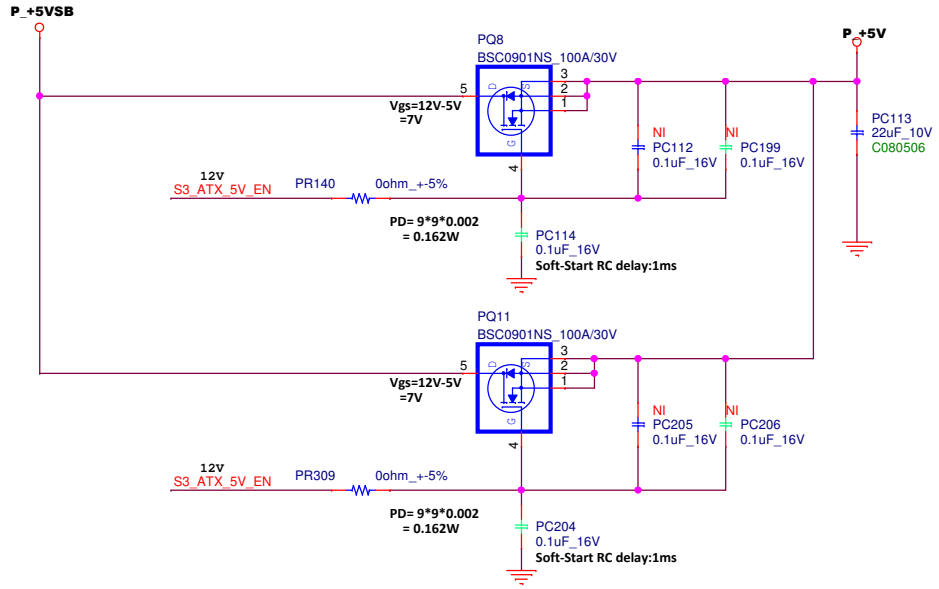
Main Power Enable Signal





P_+5V/9A

Note:
The purpose of NI of PC199 & PC206 are to fine tune
as the system shutdowns during BBU due to an unexpected deep voltage drop on P_5VSB.

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Title	P_+5V & P3.3V_SB_RGM (Load switch)	
Size: B	Document Number: COM-HPC Server Base	Rev: A1
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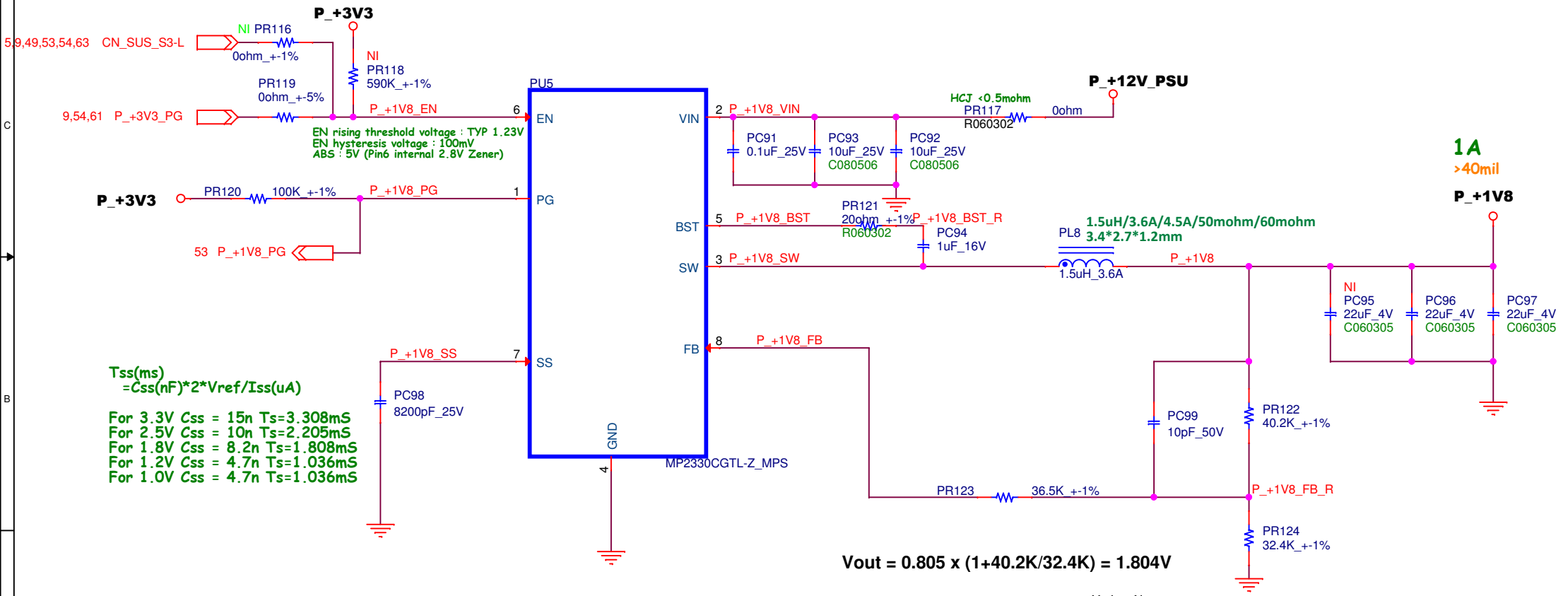
P_+1V8 (MP2330C)

P_+1V8 Specification:
Vout: 1.80V
Imax: 1A
Istep: 0.5A
Slew Rate: 1A/uS
TOB: + - 5.0%
Switching Frequency per Phase: 650kHZ



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Title	P_+1V8 (MP2330C)	
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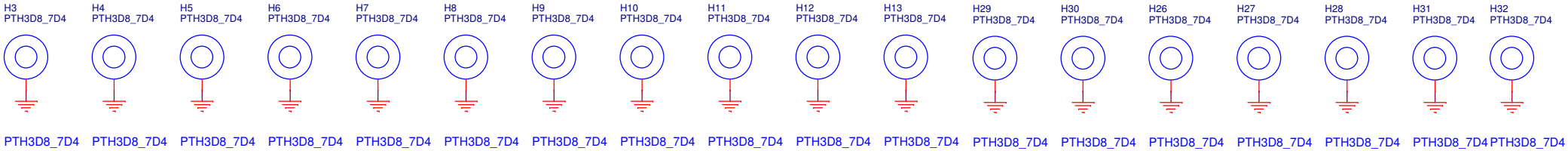
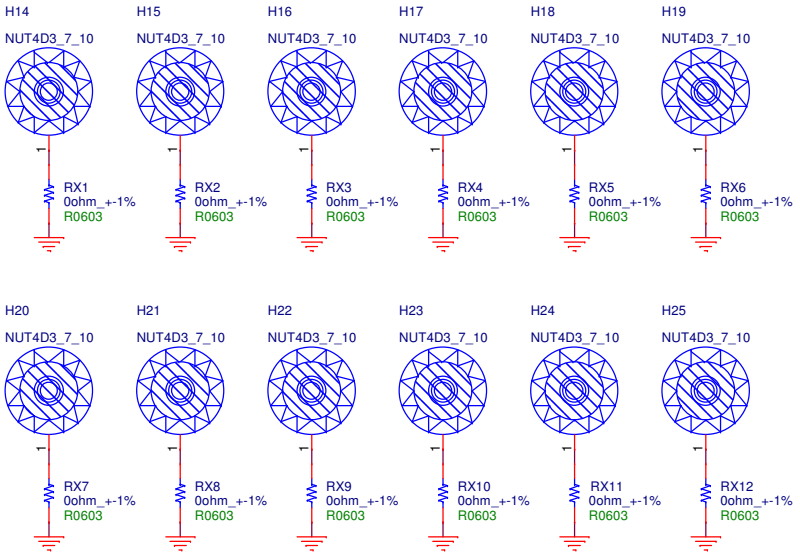
Carrier Board Screw Hole (A)

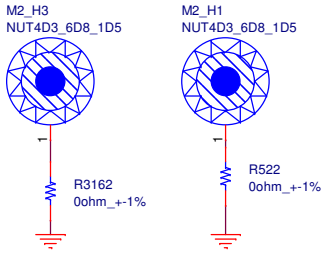


COM-Express Screw Hole (B)

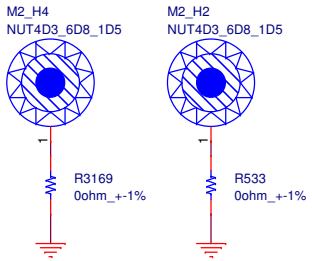


M.2 sllot Screw Hole (C)

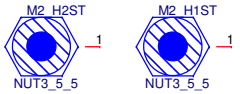
M2_1
80:M2_H2
110:M2_H4



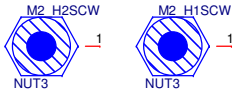
M2_0
80:M2_H1
110:M2_H3

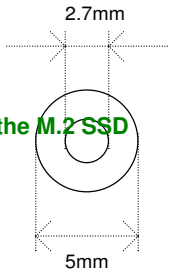


Pre-install : Standoff (33-70003-2000) for the M.2 SSD

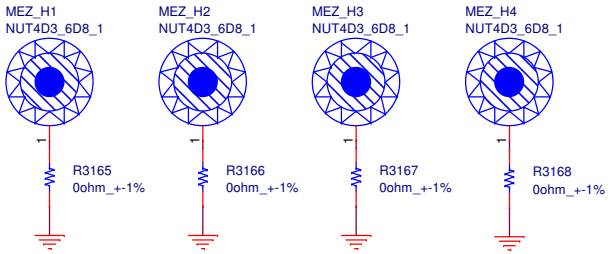


Pre-install :screws (33-03340-0040-B0) for the M.2 SSD





Mezz Board Screw Hole (D)



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A2 BOM change

	Description	Comment
1	Depop PR139	S3_ATX_5V_EN disconnect to PSU_PSON-L.
2	Depop PR98, PR102 / Pop PR325 / PR110 change to 10K	P_+1V15_BMC_AUX chage power solution
3	Depop PR76	P5V_PGOOD double PD.
4	PR36 change to 10K	Change value of pull up RES of P_+3V3_PG .
5	H14 - H25 change to 33-72186-0100-A0	Module 12PCS P/N of stand off (H14-H25) from 33-72045-0100 change to 33-72186-0100-A0 by ME request (Bottom mounting).
6	25-14001-1020 / 25-12001-1020 change to 25-10051-1020	Mini jumper change to black color by PM request.
7	Depop R120, R3521, R3526	Double Pull up.
8	21-6710E-2120 change to 21-61100-2120	Front panel pin header P/N change.
9	U20 U22 change to 73-09517-00W0	M.2 SMbus slot function
10	R885 (64-43025-4490/RES 43Kohm 0402) chage to C3260 (78-10521-C400/1uF/16V K 0402)	for BMC reset isseue when Module Power on (MOS DS gate leackage 5VCC_SB to P_+5V, RC delay for G gate enable)

A1 to A2 difference item

	Description	Comment	Pag
1	How to support 25GbE per lane (KR can up to 25) ? - OCP 3.0 connector support to 25GbE/pin ? - Fina a high speed connector, this may be a solutuon ? - A2 需確認ALT KR LAN設計相關 CEI?? redriver???? COST??	[HW_0709] OCP 3.0 connector 為夾板式botton side 容易計構干涉, R/A 可考慮 SAMTEC Board to Board connector 價格昂貴, LAN card cost up, 建議使用PCIe x16 Gen 5 slot 常用料(32Gbps/LANE) 168pin [PM 0723] Keep A1 OCP2.0 connctor and support 10GBase-KR only. Need to add 10G KR/SFI mux and retimer. Delete carrier 原先for CEI預留的IO/I2C Expender	39,40, 41,42
2	Shift the 2nd PCIe slot location (otherwise, we can't insert two GPU card) - If we don't need OCP style card, then, we can consider 3x16 PCIe card !!!	[HW_0709] x8 slot 與x16 slot 對調layout 走線影響過大, 建議x8 slot 更改為x16 slot [PM_0715] check x4 slot 常用卡長度 [HW_0721] 已請ME確認M.2干涉問題 [HW_0813] Modify PCIe slot configuration follow PM request 板邊x16 slot只support Half length PCIe card or 短卡較有穩會執行 需確認M.2 slot是否考量 heatsink高度改low profile? (Top side placement 空間受限) PCIe 走線粗估Total需增加14PCS PCIe redriver (Unit cost: USD 2.38) [PM_0816] PCIe placement如機構提供, M.2 slot 修改為low profile, 刪除部分pin header 請ME 提供DXF [ME_0922]DXF更新	20,23, 24,26, 27, 30
3	At A2 stage, we need add HW monitor for FAN control. Please must add it, 一個connector support 多個風扇 Fan control (if module thermal solution need 2 or 3 FAN, 我們不可能分開插)	[HW_0709] 需與thernal team討論SPEC 目前thermal solution為water cooling與一組tech串接3顆FAN [PM_0715] 確認使用目前thermal solution	45
4	Intel Ice Lake-D requires Quad SPI mode for the integrated 10G LAN. Carrier needs to be change to Quad SPI mode.	[HW_0709] Need to add SPI Mux and level shift for support quad SPI [PM_0715] 同意導入	48
5	USB port re-assignment - we support 8x USB port (connectors or header or whatever), but, most of server module will only support 4x USB !	[PM_0715] 1 to 4 port USB hub+redriver to 19pin connector and BMC?????USB 2.0 to wafer for test?? [PM_0723] Add 1 to 6 USB3.2 Gen2 Hub (USB7206T-I/KDX_MICROCHIP) Hub to front USB connector 走線過長需加redriver	32, 33, 34, 35
6	Jumper color 全部換黑色	PM request ,P/N change to 25-10051-1020	
7	Module Type detect: Server Module – Fixed 12V input for AT power PSU only, 不滿足ATX PSU	[PM_0715] Module type check support AT PSU only, add 1x4Pin header for Module 5VSB.	53, 62
8	Design M.2 HDD LED for Front panel header		47
9	Botton mount, 螺柱 12PCS 換料	[ME_0813] ME 換料Bottom mounting 33-72186-0100-A0 SMT Support,through,Ø2.7,H10 HONGYANG_B-14061-24 使用數量: 12	65
10	Carrier PCB mounting hole 位置修改, follow ALT chassis	ME 請Check 是否符合E-ATX spec 9/27 ME 更新DXF導入新增兩個孔位與移動一個孔位	
11	ADLINK LOGO	[HW_1012]提供文字面for PM review.	
12	組裝 carrier into the chassis, 我們會看到 文字面是顛倒的 比如說你去看PCIe 插槽文字面 請A2時候, 上下反轉一下, 位置不用動	[HW_1012]提供文字面for PM review.	
13	P_+3V3SB power solution更換成TPS53319	[PJM_1018] PJM反應缺料更換Power IC. [Power_1019] 更新線路for layout routing	55
14	Remove names and the silkscreen boxes around minor components	[PM_1019] 零件邊寬移除 [HW_1020] 與製程確認規則如下 1. SMT: BGA/CSP 零件 2. DIP: 所有DIP 零件都保留文字框, 以供人員插件時作業方便及避免方向插錯. 部分DIP 件背面有使用白漆分隔PTH以減少短路, 也請保留. 3. 指撥開關Switch (Pin 1 標示) [PM_1020]確認同意	

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