CONTENTS

Page List

A2 Modify:
1. Change page14 content to SMART-BATTERY-POWER
2. Change page15 content to 5V_AND_3.3V_AUX_POWER_SUPPLY
3. Add page20 with content VCC5V0_STB_POWER_SUPPLY
4. Add page21 with content DC_IN_12V_POWER_SUPPLY
5. Shunt table update
   Correct P/N to 25-14001-1020
   Correct DESCRIPTION to 2.54mm pitch
   Add JPX1-5 location and updated total quantity to 12
6. Add SMBUS address tabel
7. Change Page 16 content to 1.5V POWER SUPPLY

SHUNT TABLE

P/N	QUANTITY	DESCRIPTION	LOCATIONS
25-14001-1020	13	CONN, SHUNT, 2.54MM PITCH, ROHS	JP1 - SHUNT "S_JP1" BRIDGES PIN 1-2 JP2 - SHUNT "S_JP2" BRIDGES PIN 1-2 JP3 - SHUNT "S_JP3" BRIDGES PIN 1-2 JP4 - SHUNT "S_JP4" BRIDGES PIN 1-2 JP5 - SHUNT "S_JP5" BRIDGES PIN 1-2 JP6 - SHUNT "S_JP6" BRIDGES PIN 2-3 JP7 - SHUNT "S_JP7" BRIDGES PIN 1-2 JPX1 - SHUNT "S_JPX1" BRIDGES PIN 2-3 JPX2 - SHUNT "S_JPX2" BRIDGES PIN 1-2 JPX3 - SHUNT "S_JPX3" BRIDGES PIN 1-2 JPX4 - SHUNT "S_JPX4" BRIDGES PIN 1-2 JPX5 - SHUNT "S_JPX5" BRIDGES PIN 1-2 JPX8 - SHUNT "S_JPX8" BRIDGES PIN 1-2
25-10013-1020	1	CONN, SHUNT, 2.00MM PITCH, ROHS	JPX7 - SHUNT "S_JPX7" BRIDGES PIN 1-2

SMBus Address

Device	Address
ETH1	63h
9DB403	43h
9DB433	DCh / DDh
AD5301	1Ah
IO EXPENDER	42h
MINI-PCIE1	NA
MINI-PCIE2	NA

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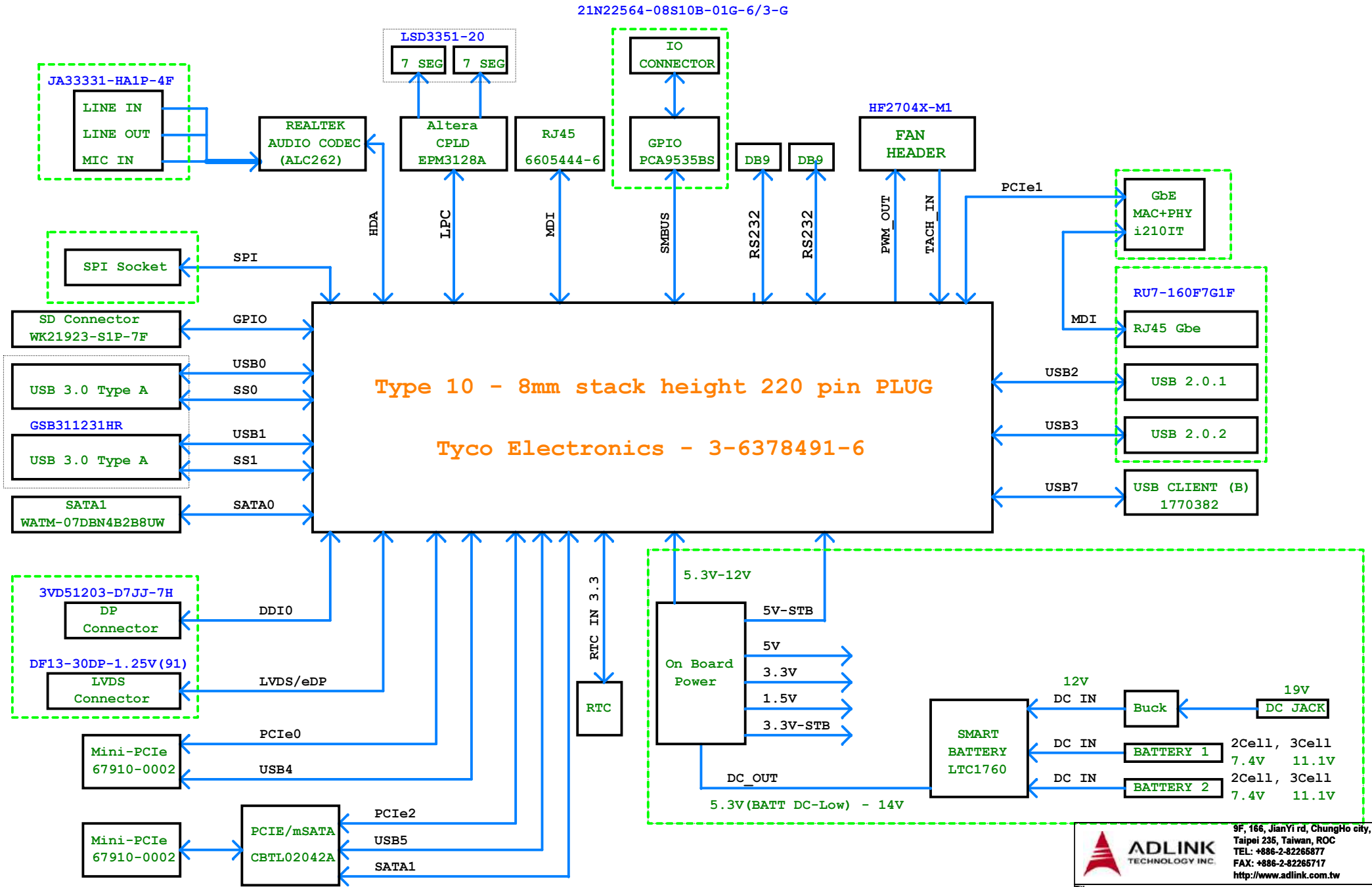
BLOCK DIAGRAM



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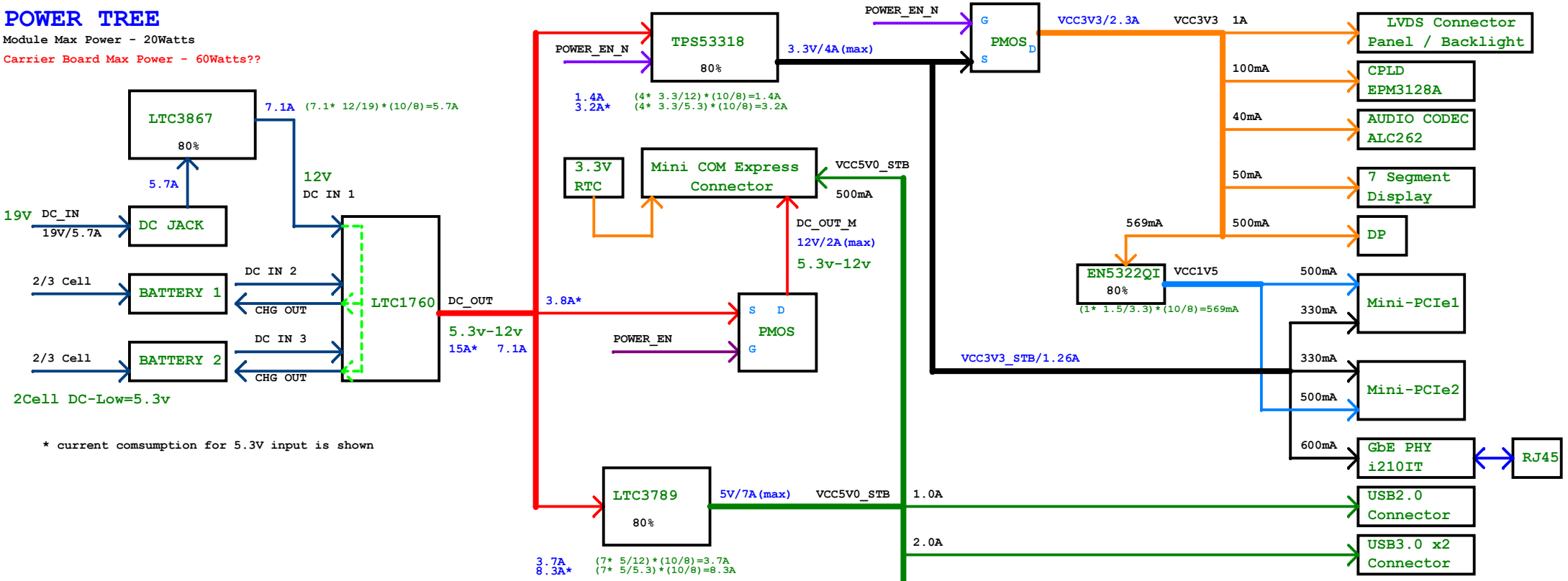
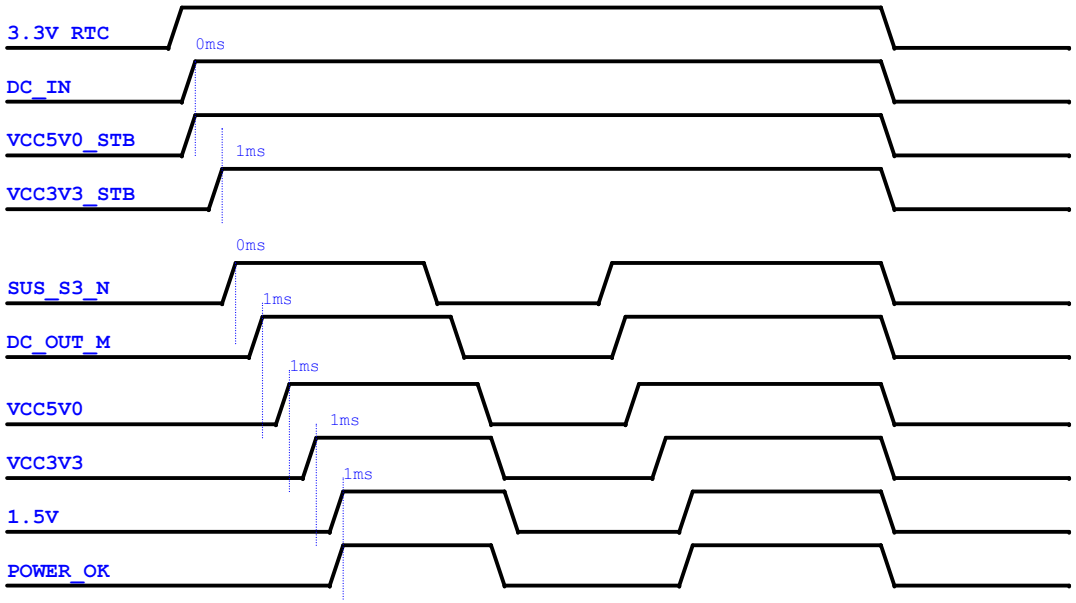
POWER TREE

Module Max Power - 20Watts

Carrier Board Max Power - 60Watts??



POWER SEQUENCE



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Title		
POWER & RESET SCHEME		
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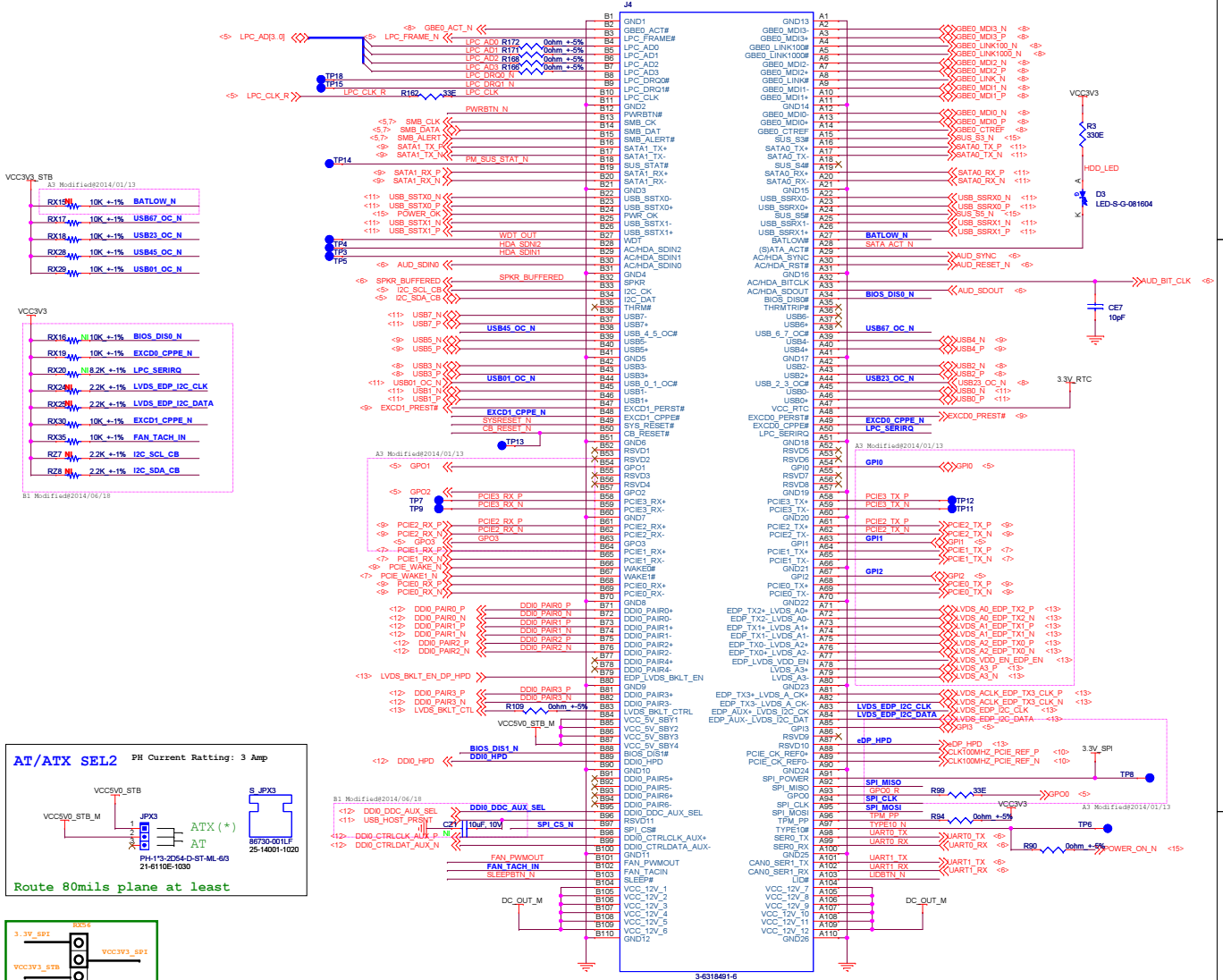
COM EXPRESS TYPE 10 CONNECTOR

TYPE 10 BASE BOARD CONNECTOR



AT/ATX SEL2

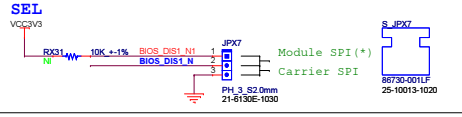
PH Current Ratting: 3 Amp

Route 80mils plane at least

SPI socket

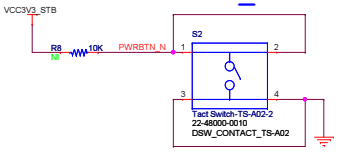
SPI P/N: 71-09112-0010

SPI SEL

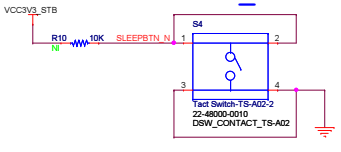


BIOS_DIS0#	BIOS_DIS1#	SPI SEL
1	1	Module SPI
1	0	Carrier SPI

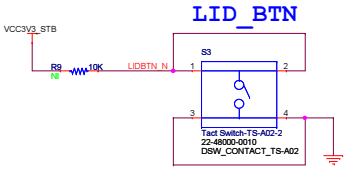
POWER_BTN



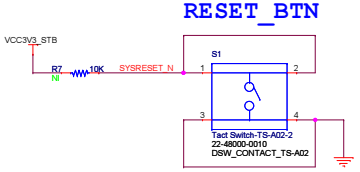
SLEEP_BTN



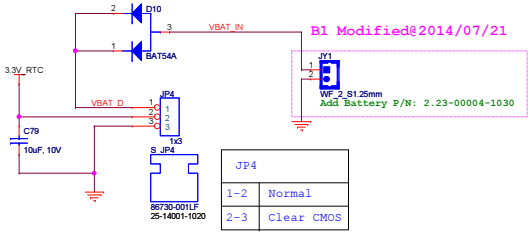
LID_BTN



RESET_BTN

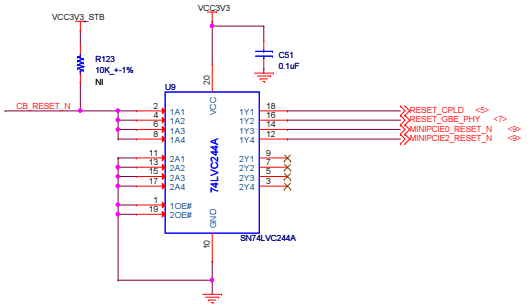


RTC BATTERY HOLDER

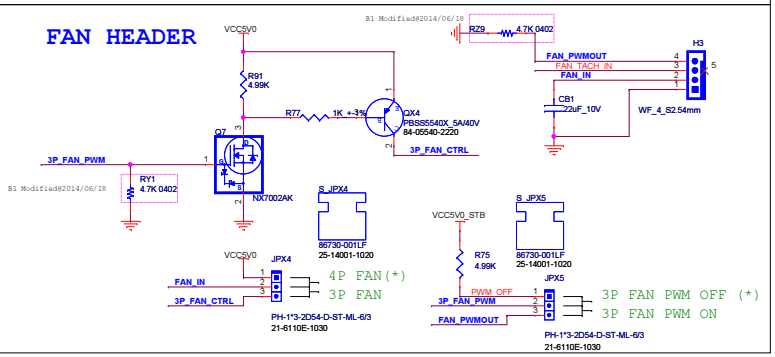


JP4	
1-2	Normal
2-3	Clear CMOS

BASE BOARD RESET



FAN HEADER



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Title: TYPE 10 COM EXPRESS CONNECTOR

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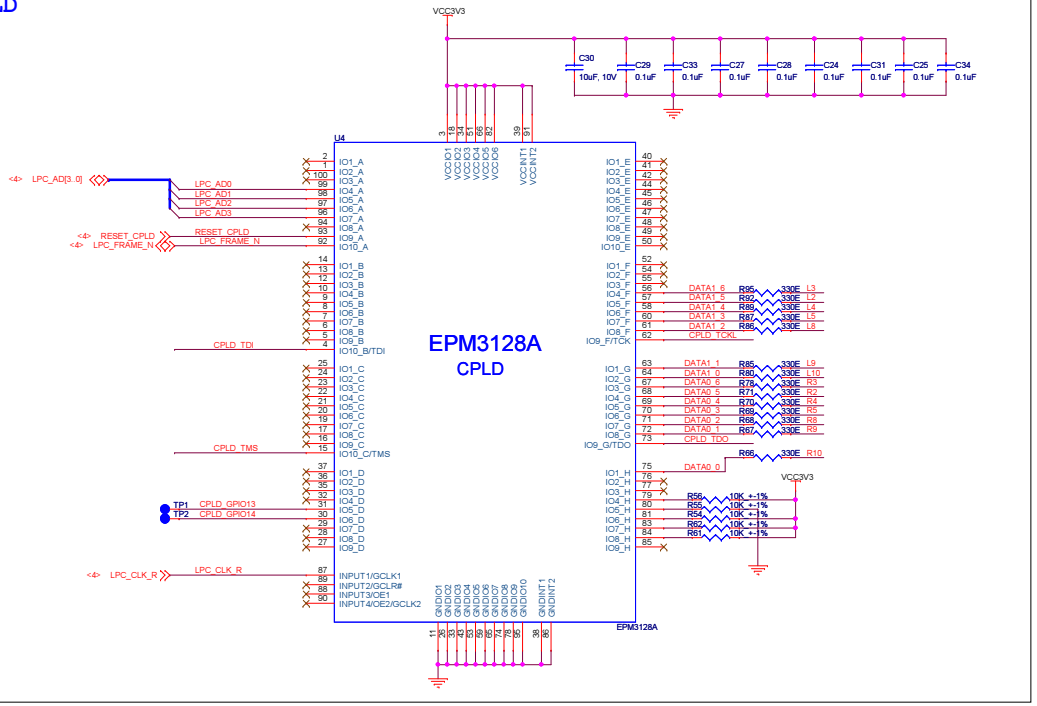
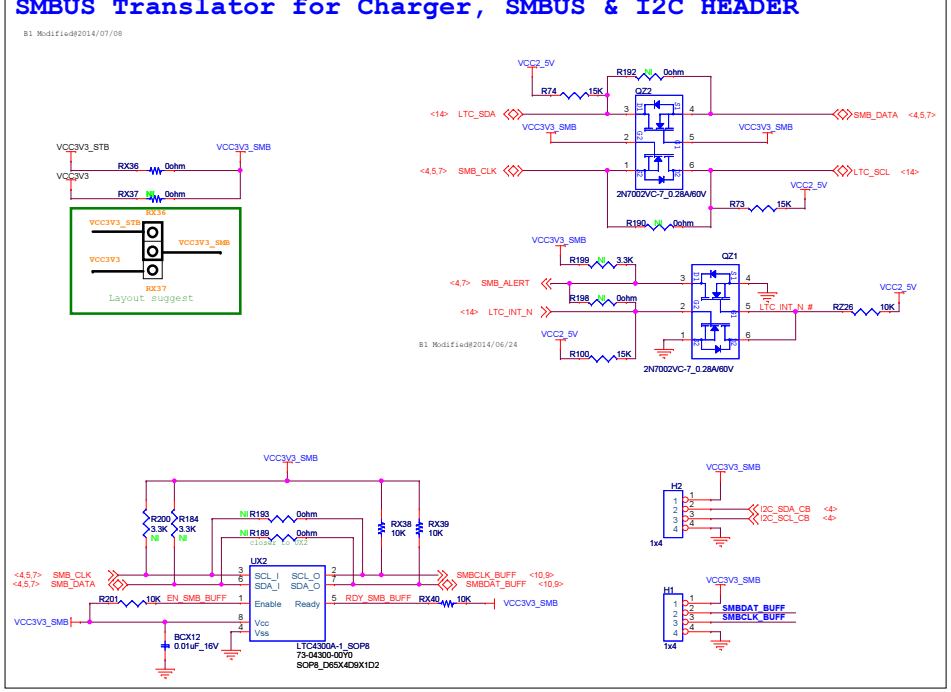
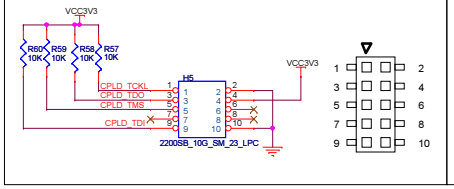
CPLD



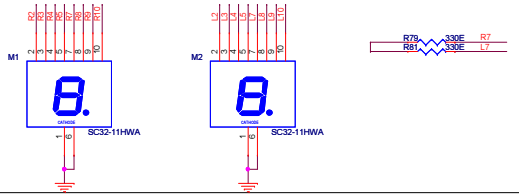
SMBUS Translator for Charger, SMBUS & I2C HEADER



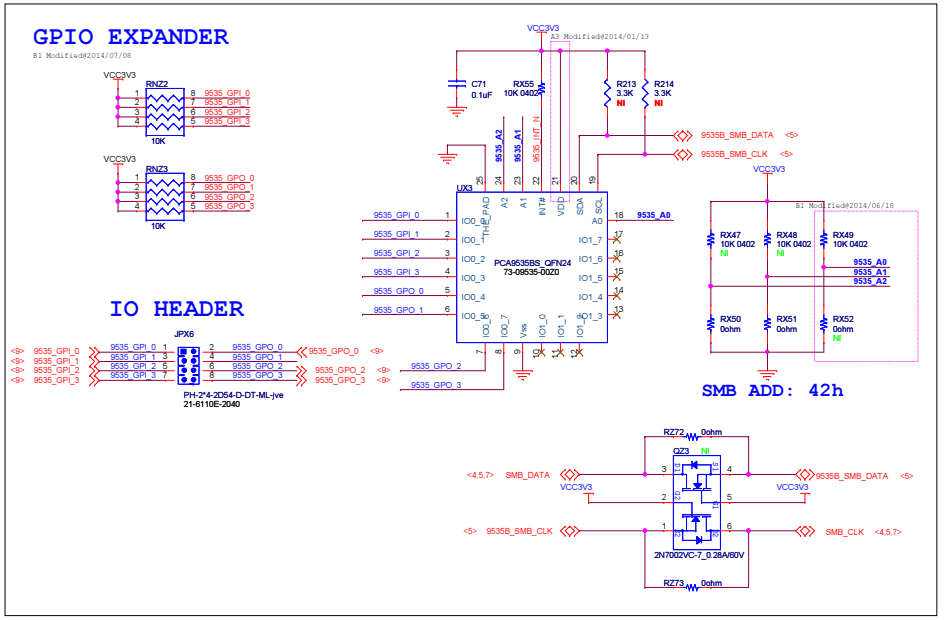
CPLD JTAG



SEVEN SEGMENT LED

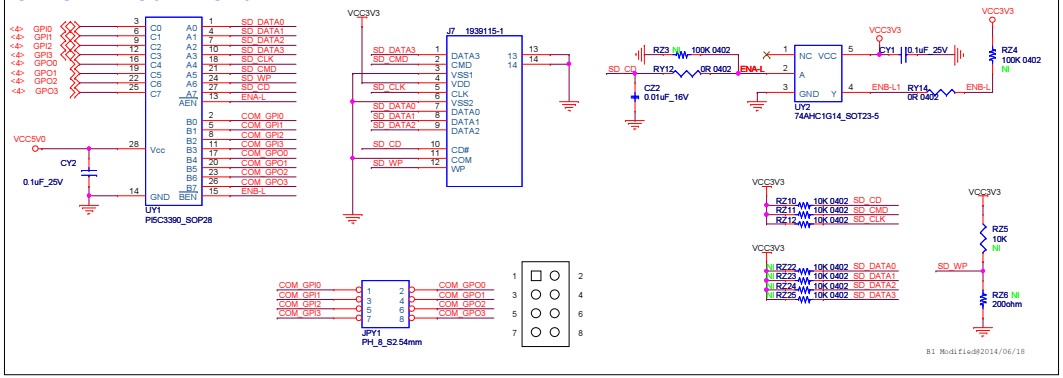


GPIO EXPANDER



IO HEADER

SD CARD CONNECTOR



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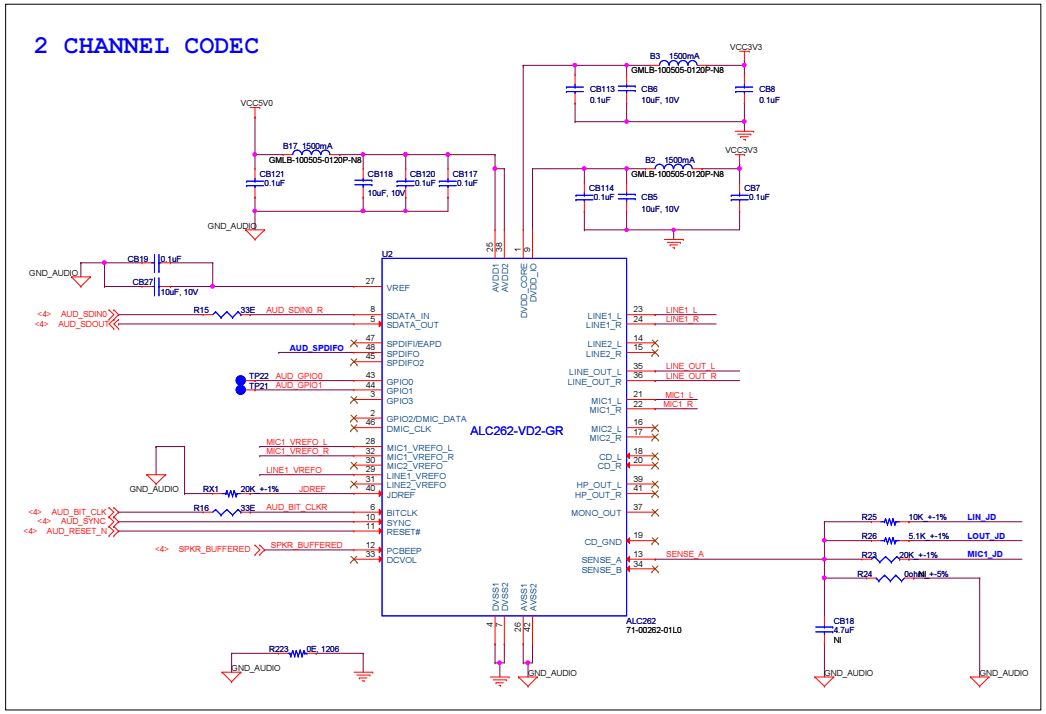

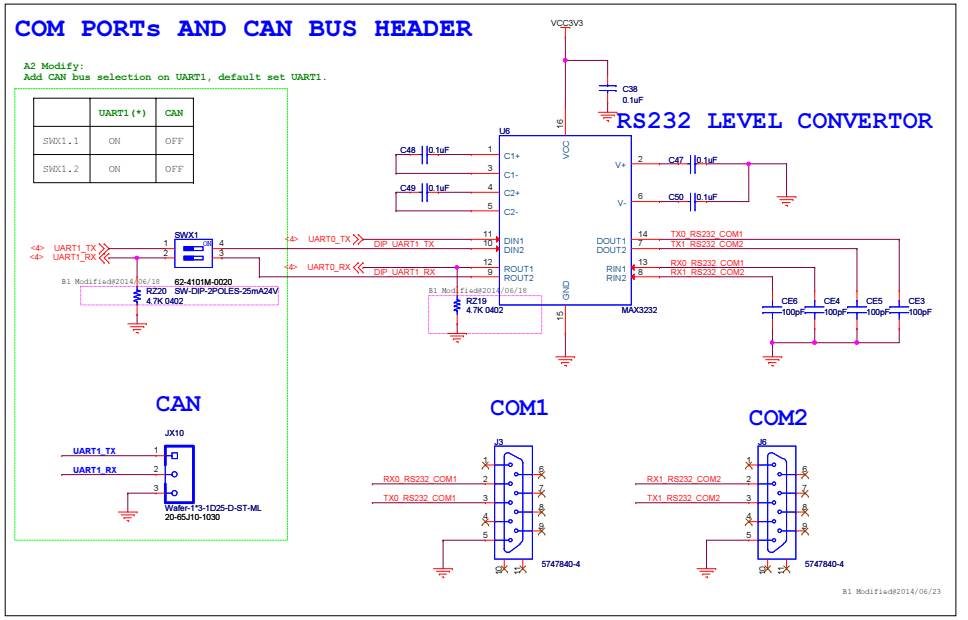

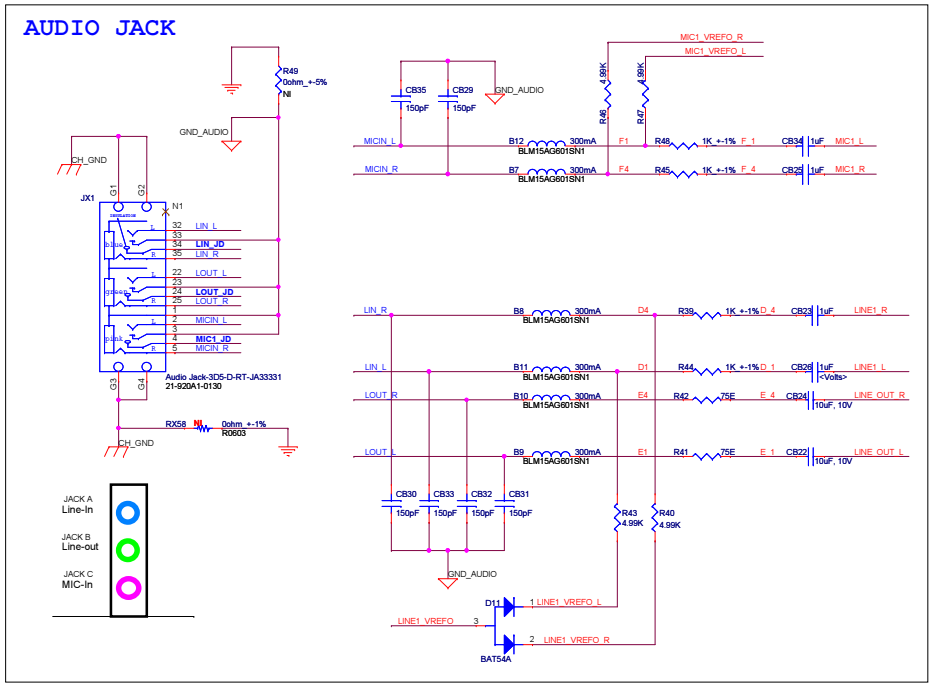

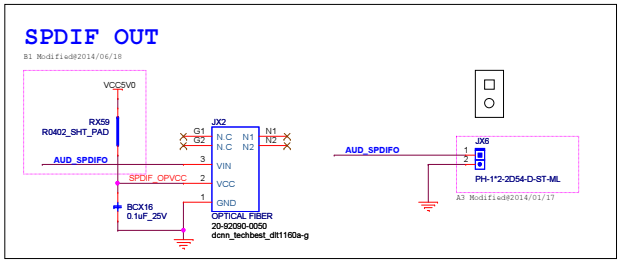

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Title	AUDIO CODEC
Size	A2
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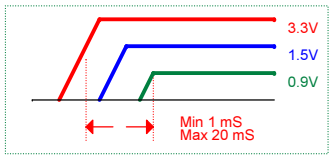
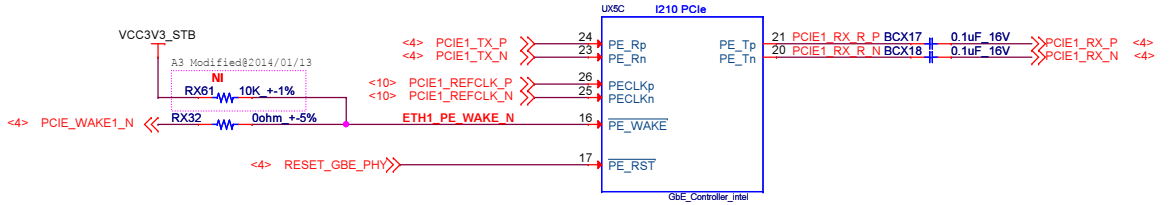
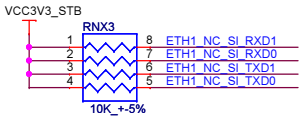
PCIE BASED MAC+PHY (ETHERNET1)

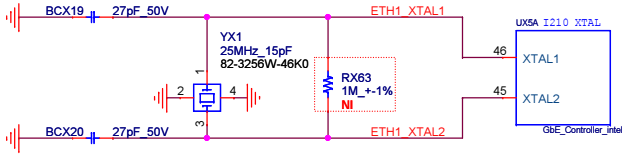
Power Sequencing

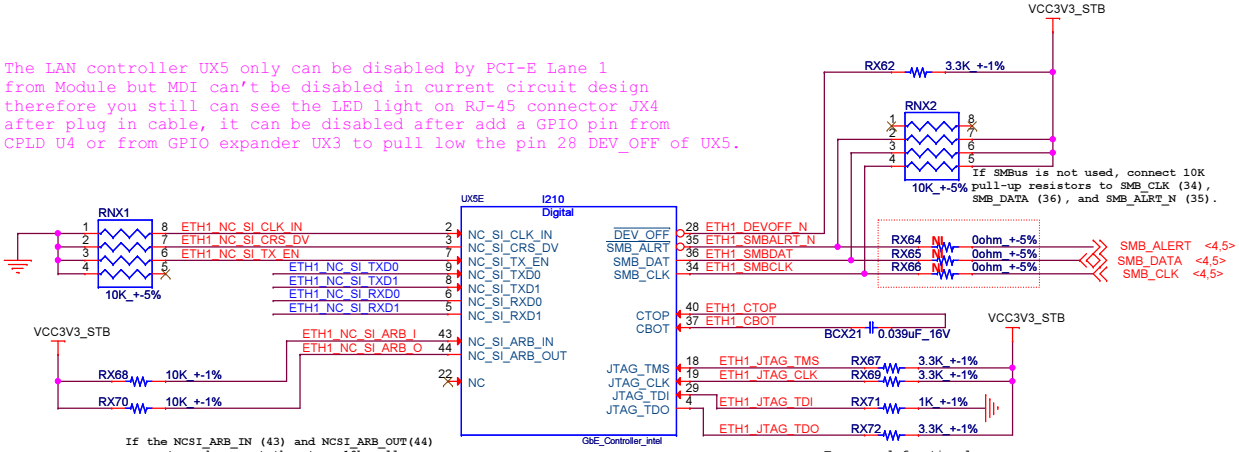


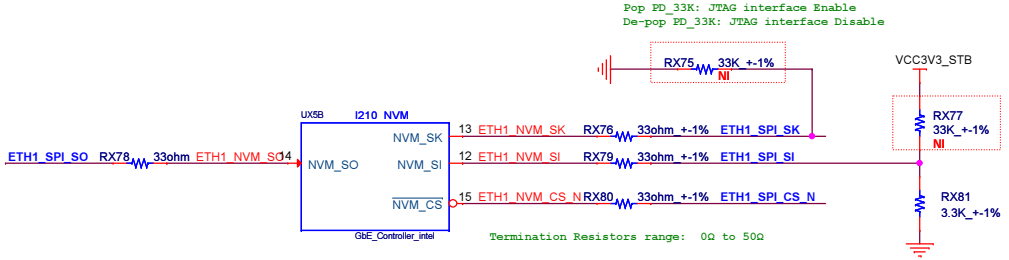


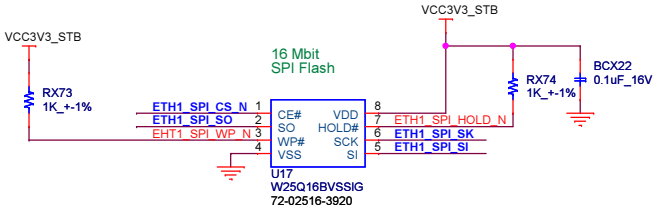
The LAN controller UX5 only can be disabled by PCI-E Lane 1 from Module but MDI can't be disabled in current circuit design therefore you still can see the LED light on RJ-45 connector JX4 after plug in cable, it can be disabled after add a GPIO pin from CPLD U4 or from GPIO expander UX3 to pull low the pin 28 DEV_OFF of UX5.

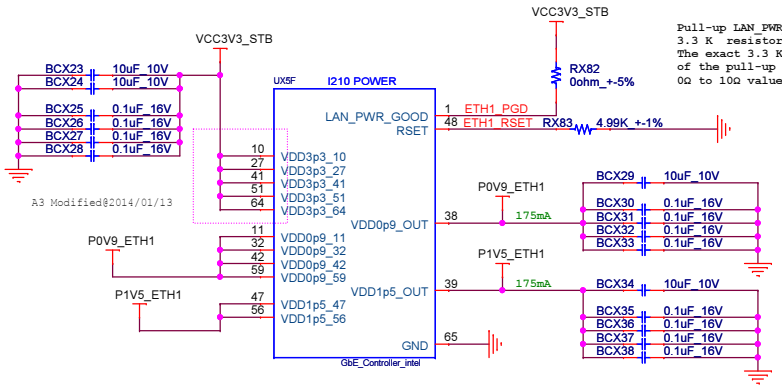


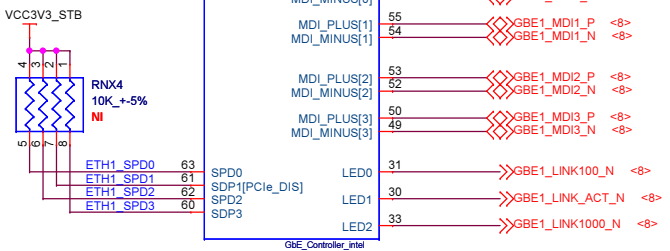


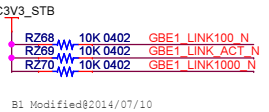












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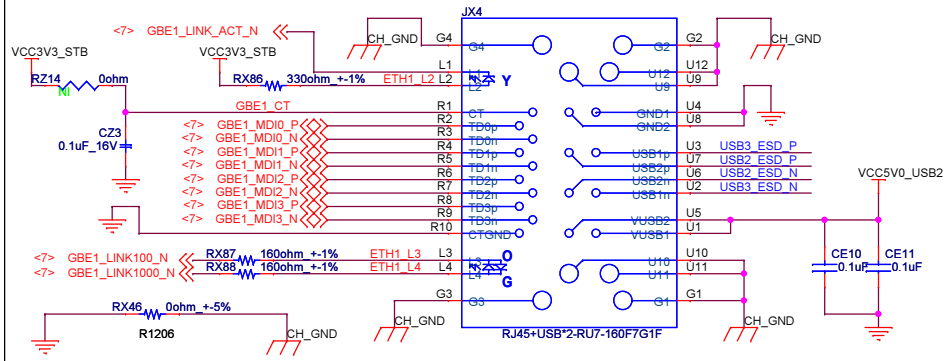
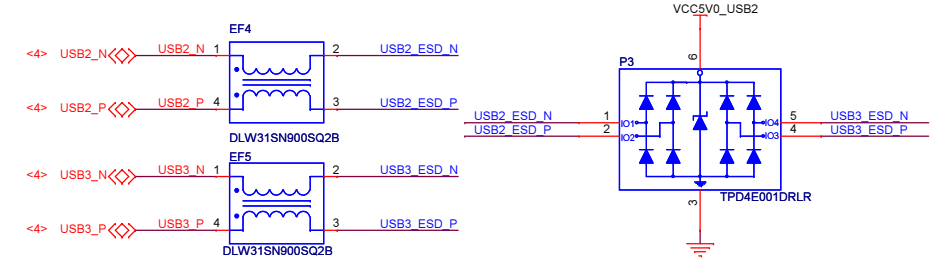
Ethernet Jack1 (Carrier) and Dual USB2.0 Connector

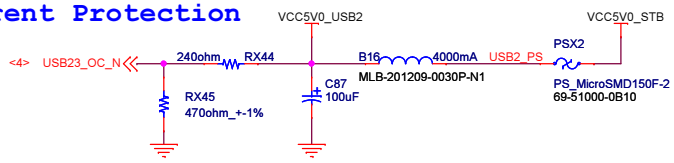
B1 Modified@2014/06/18



USB ESD & COMMON MODE CHOKE

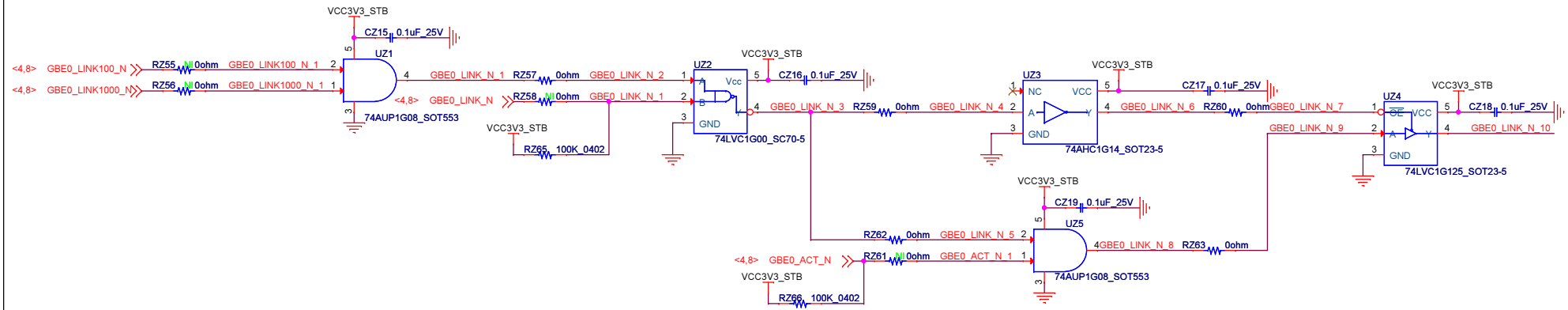


USB Current Protection

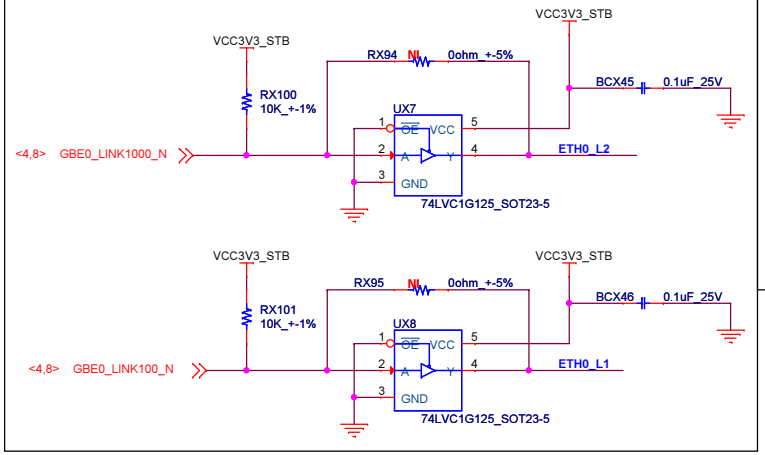


RJ-45 Receptacle (ACT-LED) for Ethernet Jack0 (Module)

B1 Modified@2014/07/09

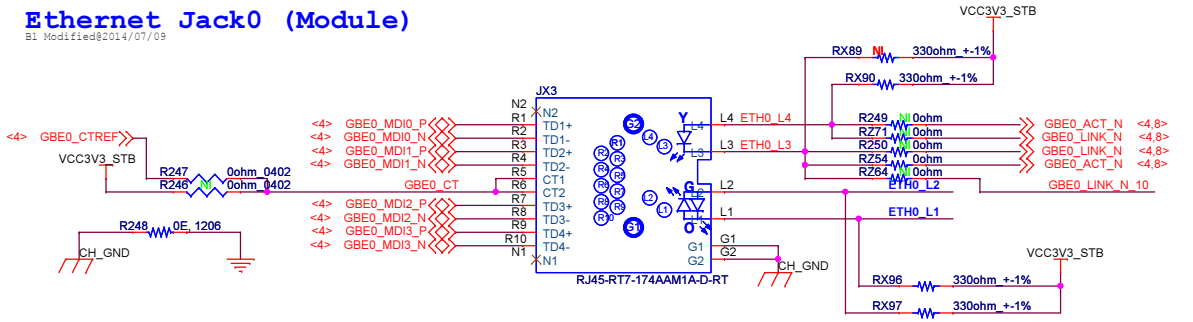


Ethernet Jack0 (Module) 100/1000 Select



Ethernet Jack0 (Module)

B1 Modified@2014/07/09



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Title		
RJ45 CONNECTORS		
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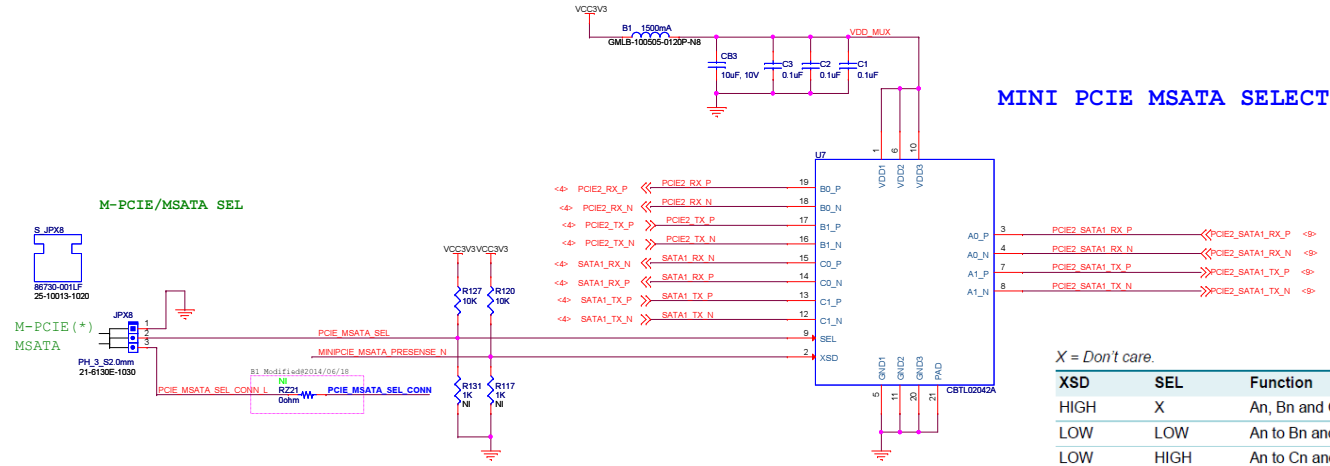
MINI PCIE CONNECTORS



X = Don't care.

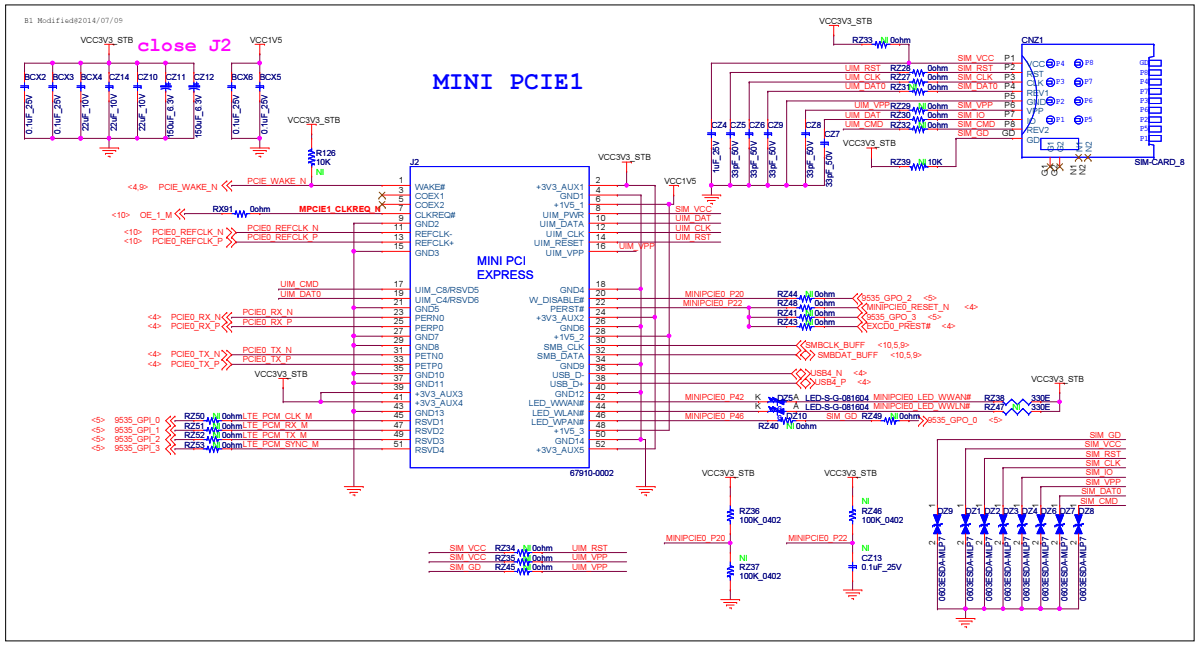
XSD	SEL	Function	
HIGH	X	An, Bn and Cn pins are high-Z	(DEFAULT)
LOW	LOW	An to Bn and vice versa	(mini-PCIe)
LOW	HIGH	An to Cn and vice versa	(mSATA)

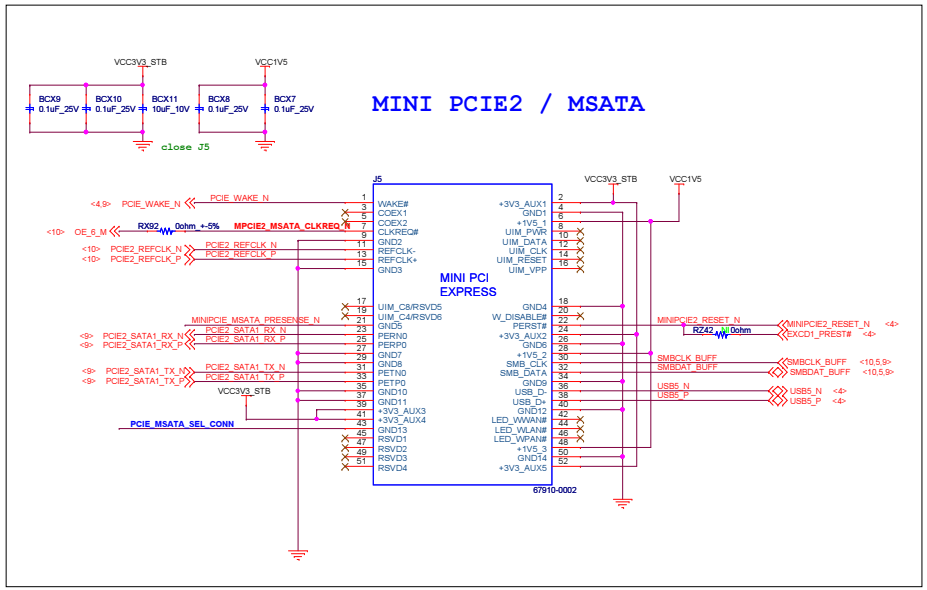
mSATA Receiver differential signal pair define is different to mini-PCIe connector difine. (should be swap on U7 input)

P23	+B	Host Receiver Differential Signal Pair
P24	+3.3V	3.3V Source
P25	-B	Host Receiver Differential Signal Pair

mSATA pin define for XSD(P21) and SEL(P43)

P21	GND	Return Current Path
P43	Device Type	Shall be a No Connect on mSATA Devices[4]





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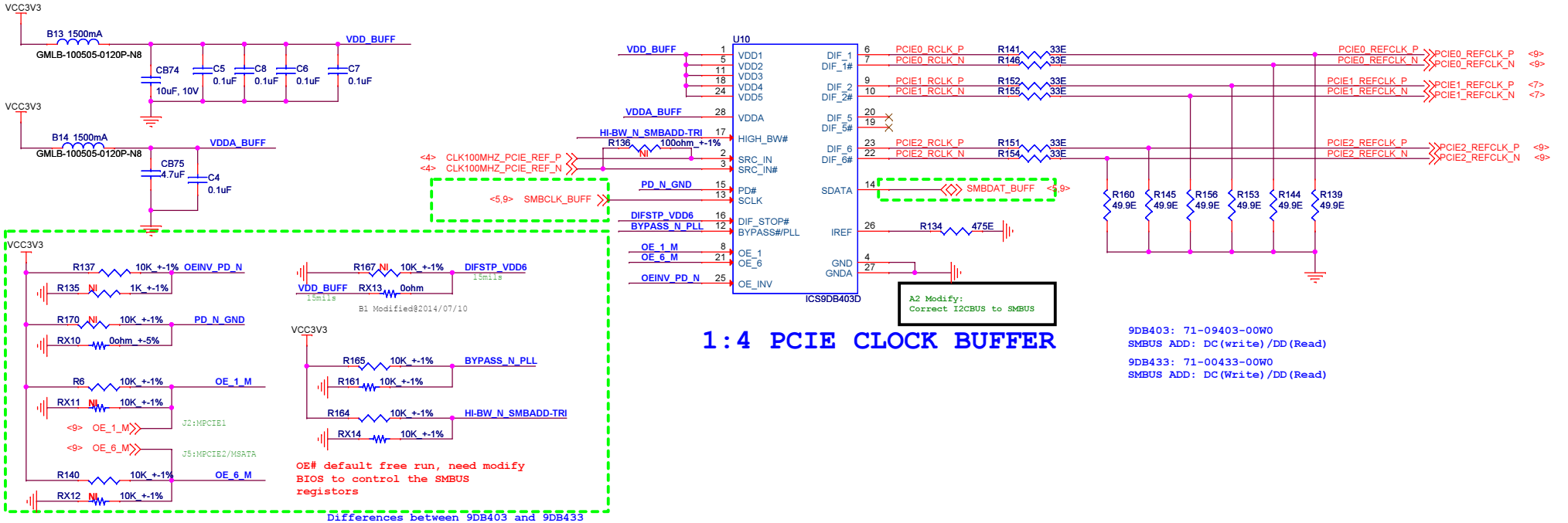
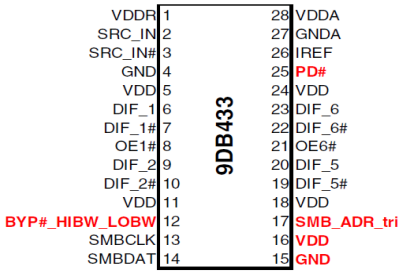
CLOCK BUFFER AND SD CARD CONNCTOR



1:4 PCIE CLOCK BUFFER

9DB403: 71-09403-00W0
SMBUS ADD: DC(write)/DD(Read)

9DB433: 71-00433-00W0
SMBUS ADD: DC(Write)/DD(Read)



Differences between 9DB403 and 9DB433

9DB403

Pin12: 0 = Bypass mode, 1= PLL mode

Pin15: Pull down to disable the internal clocks and the VCO and stopped the crystal

Pin16: Active low input to stop differential output clocks.

Pin17: 0 = High BW, 1= Low BW

Pin25: 0 = OE pins active high, 1 = OE pins active low (OE#)

9DB433

Pin12: Low(<0.8V) = Bypass mode, Mid(1.2<Vin<1.8V) = PLL 100M Hi BW, High(Vin > 2.0V) = PLL 100M Low BW

Pin15: GND only

Pin16: VDD only

Pin17: SMBus Address Selection and Readback; Low = DA/DB, Mid = DC/DD, High = D8/D9

Pin25: Pull down to disable the internal clocks and the VCO and stopped the crystal

Strap Pin BOM SEL:	9DB403	9DB433 (default)
Pin12	BYPASS#/PLL(PLL) R161: DNP R165: POP	BYP_HIBW_LOBW(PLL 100M Hi BW) R161: POP R165: POP
Pin15	PD#(Disable) R170: POP RX10: DNP	GND R170: DNP RX10: POP
Pin16	DIF_STOP#(Disable) R167: POP RX13: DNP	VDD R167: DNP RX13: POP
Pin17	HIGH_BW# R164: POP RX14: DNP	SMB_ADR_tri(Mid) R164: POP RX14: POP
Pin25	OE_INV(OE#) R137: DNP R135: POP	PD# Disable R137: POP R135: DNP

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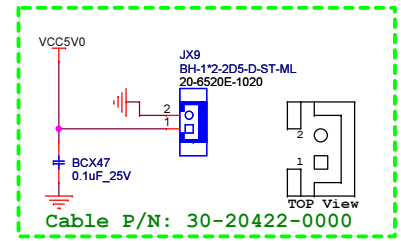
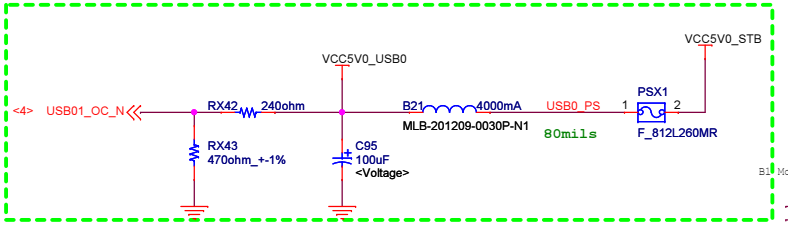
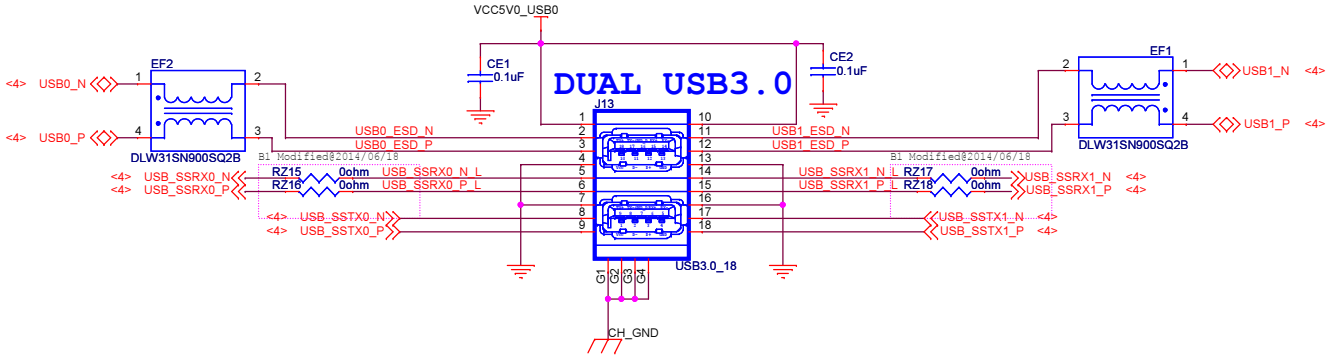
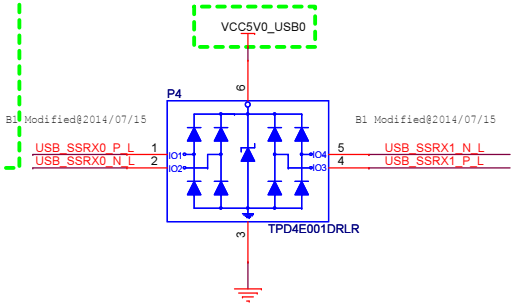
Title			
CLOCK BUFFER			
Size: A3	Document Number: MiniBase-10R		Rev: B1
Date: Monday, July 21, 2014	Sheet 10 of 21		

USB AND SATA CONNCTORS

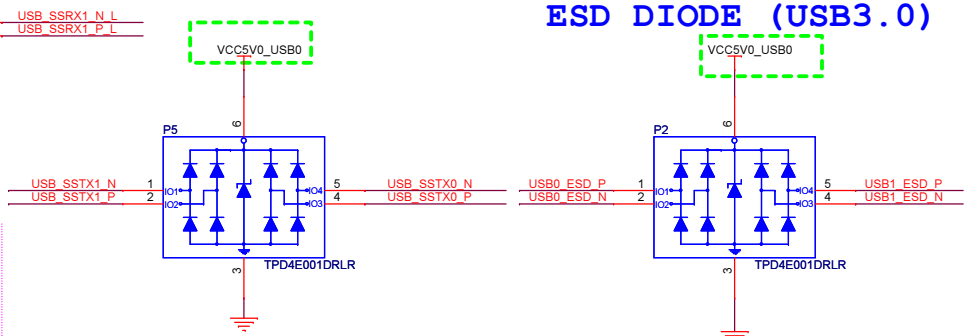




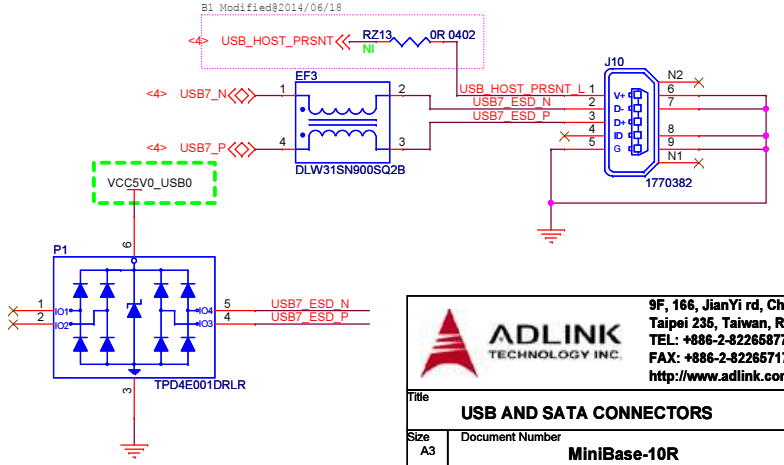


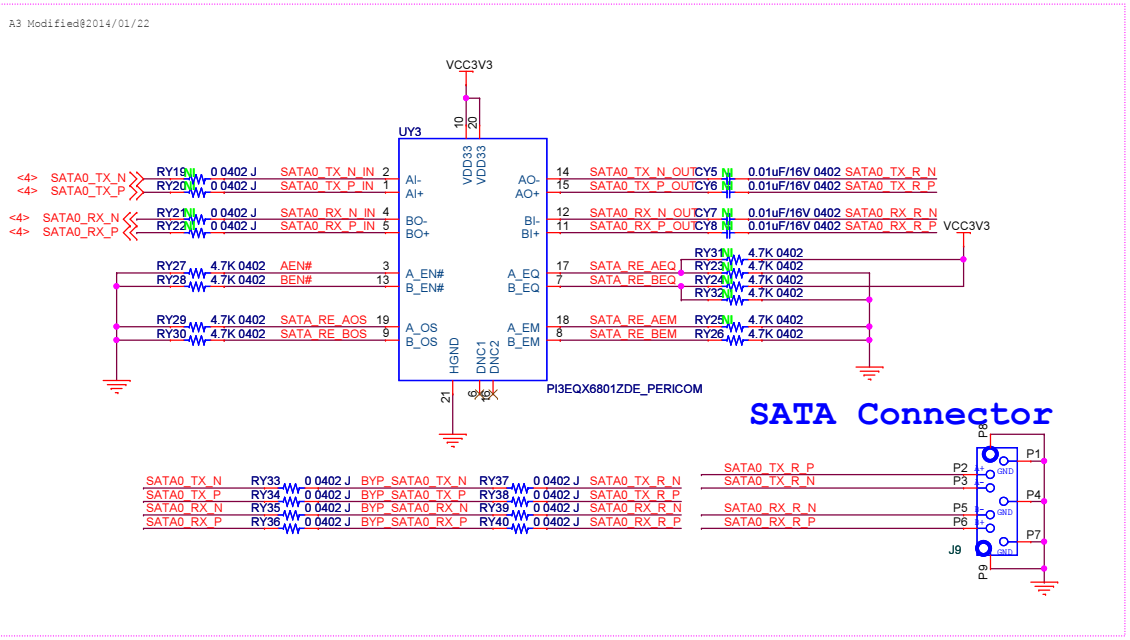


ESD DIODE (USB3.0)



MINI USB (CLIENT)





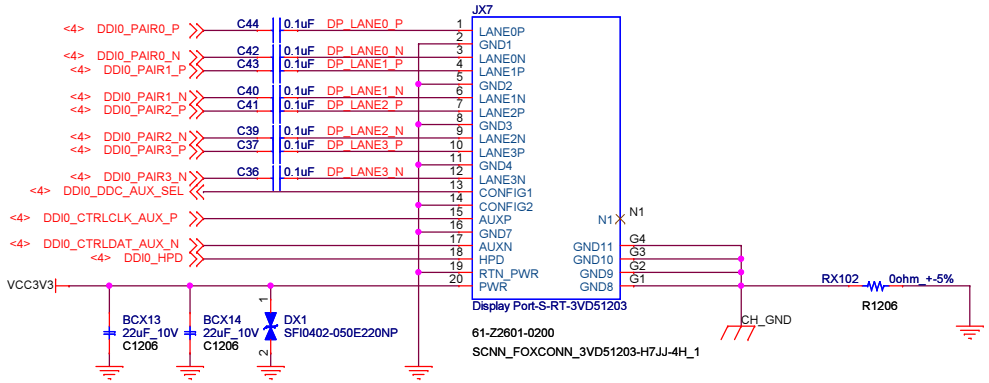
DP CONNECTOR

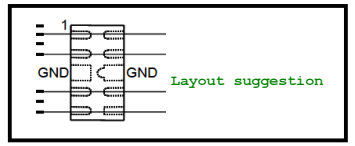
RX34 NI 1M_+-1% DDI0_DDC_AUX_SEL

Optional for DDI0_DDC_AUX_SEL (default DNP)

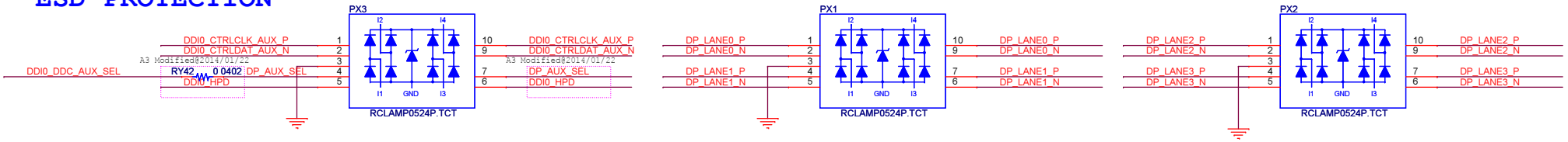
RX33 NI 100K_+-1% DDI0_HPD

Optional for DDI0 hot plut (default DNP)





ESD PROTECTION



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Title		
DP CONNECTOR		
Size: A3	Document Number: MiniBase-10R	Rev: B1
Date: Monday, July 21, 2014	Sheet 12 of 21	

A2 Modify:
Remove LVDS to HDMI item.

BOM:
Remove: J11
Remove: U13,U22,U23,U26
Remove: R178-179,R207-209
Remove: CE9,C56-57,C59,C60-62,C66-68

A2 Modify:
1. Change R216,R219,JP6.1 power source from DC_OUT_9~16V to VCC5V0
2. Change backlight 12v power design to 3.3v
3. Change net I2C_SCL to I2C_SCL_CB
4. Change net I2C_SDA to I2C_SDA_CB
5. Change J8 to JX8(61-65J05-2150)
6. Combine H8(21-6510E-2040) to JX8
7. Add 1 pin with VCC3V3 for panel EDID
8. Change R211 package size from R0402 to R0603

Panel EDID power

LVDS Backlight Control

LVDS/eDP Connector

JP3(BRIGHTNESS CONTROL)	
1-2	Voltage level
2-3	PWM

For eDP function, RY2~RY7, RY10~RY11, RZ1~RZ2 should be 78-10423-2450 (0.1uF,0402)

Optional for eDP hot plut (default DNP)

JP5(PNL POWER)	
1-2	3.3V
2-3	5.0V

JP6(BKLIGHT POWER)	
1-2	3.3V
2-3	5.0V

JY2(eDP Backlight Connector)	
2cell	6~12V
3cell	9~14V

BRIGHTNESS CONTROL

I2C ADD: 0001101b (0x1Ah)

JP7(BRIGHT PWM SOURCE)	
1-2	GPU
2-3	LVDS I2C

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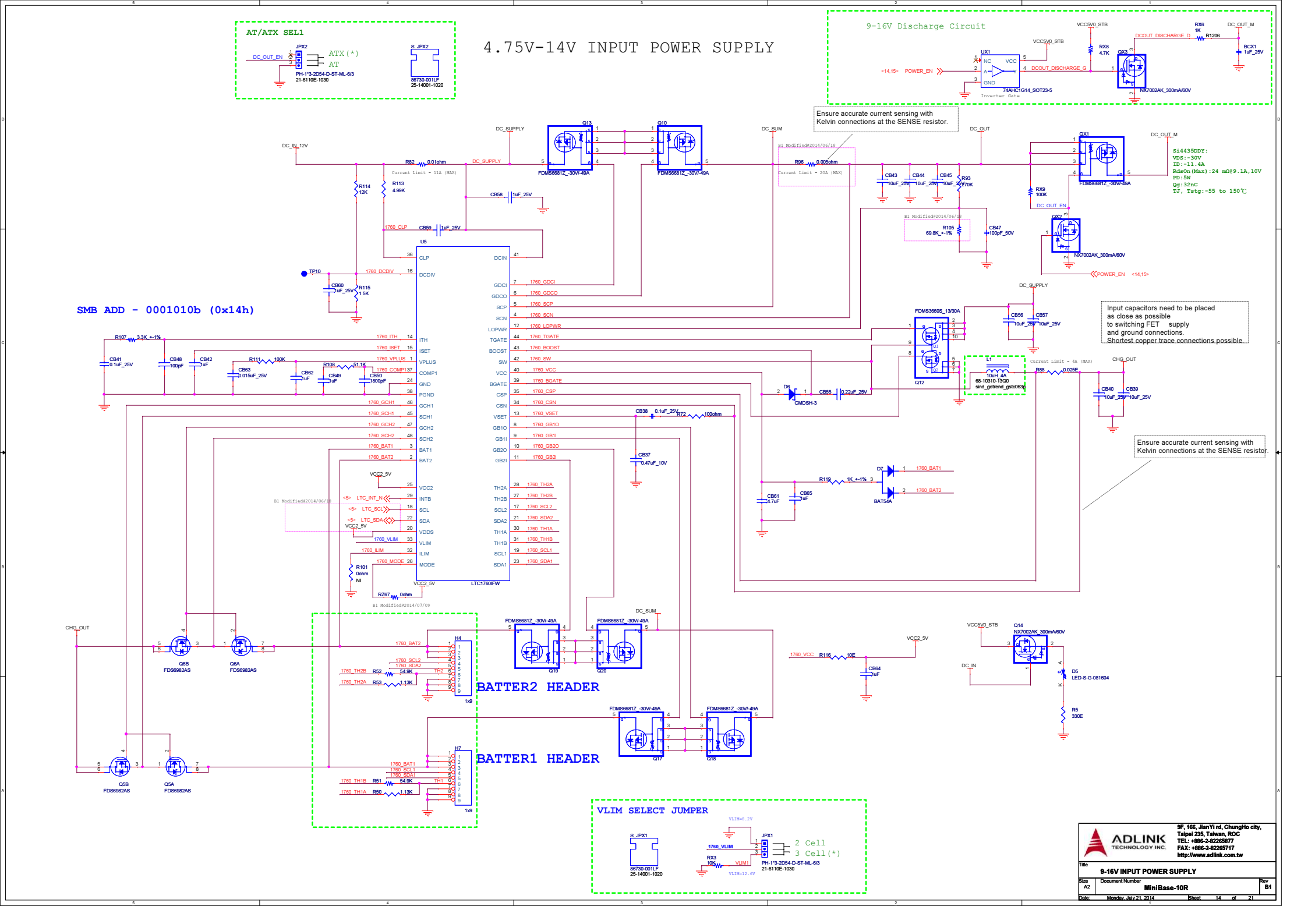
Title: HDMI CONNECTOR
Size: A2 | Document Number: MiniBase-10R | Rev: B1
Date: Thursday, October 09, 2014 | Sheet 13 of 21


4.75V-14V INPUT POWER SUPPLY
AT/ATX SEL1
JPX2
ATX(*)
AT
DC_OUT_EN
PH-1*3-2D54-D-ST-ML-6/3
21-6110E-1030
S_JPX2
86730-001LF
25-14001-1020
9-16V Discharge Circuit
VCC5V0_STB
RX6 1K
DC_OUT_M
R1206
BCX1 1uF_25V
RX8 4.7K
QX3
DCOUT_DISCHARGE_D
DCOUT_DISCHARGE_G
UX1
74AHC1G14_SOT23-5
Inverter Gate
NX7002AK_300mA/60V
POWER_EN
Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
DC_IN_12V
DC_SUPPLY
DC_SUM
DC_OUT
Q13
Q10
FDMS6681Z_-30V/-49A
R82 0.01ohm
Current Limit = 11A (MAX)
R96 0.005ohm
Current Limit = 20A (MAX)
R114 12K
R113 4.99K
CB58 1uF_25V
CB59 1uF_25V
1760_CLP
U5
LTC1760IFW
CB43 10uF_25V
CB44 10uF_25V
CB45 10uF_25V
R93 470K
QX1
Si4435DDY:
VDS:-30V
ID:-11.4A
RdsOn(Max):24 mΩ@9.1A,10V
PD:5W
Qg:32nC
TJ, Tstg:-55 to 150℃
RX9 100K
DC_OUT_EN
QX2
NX7002AK_300mA/60V
R105 69.8K_+-1%
CB47 100pF_50V
TP10
CB60 1uF_25V
R115 1.5K
1760_DCDIV
SMB ADD - 0001010b (0x14h)
R107 3.3K +-1%
CB41 0.1uF_25V
CB48 100pF
CB42 1uF
R111 100K
CB63 0.015uF_25V
CB62 1uF
R108 51.1K
CB49 1uF
CB50 1800pF
1760_ITH
1760_ISET
1760_VPLUS
1760_COMP1
1760_GCH1
1760_SCH1
1760_GCH2
1760_SCH2
1760_BAT1
1760_BAT2
VCC2_5V
1760_VLIM
1760_ILIM
1760_MODE
R101 0ohm NI
RZ67 0ohm
B1 Modified@2014/07/09
B1 Modified@2014/06/18
<5> LTC_INT_N
<5> LTC_SCL
<5> LTC_SDA
FDMS3660S_13/30A
Q12
CB56 10uF_25V
CB57 10uF_25V
Input capacitors need to be placed as close as possible to switching FET supply and ground connections. Shortest copper trace connections possible.
L1
10uH_4A
68-10310-13Q0
sind_gotrend_gstc063d
Current Limit = 4A (MAX)
R88 0.025E
CHG_OUT
CB40 10uF_25V
CB39 10uF_25V
D6
CMDSH-3
CB55 0.22uF_25V
CB38 0.1uF_25V
R72 100ohm
CB37 0.47uF_10V
R119 1K +-1%
D7
BAT54A
CB61 4.7uF
CB65 1uF
Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
CHG_OUT
Q6B FDS6982AS
Q6A FDS6982AS
Q5B FDS6982AS
Q5A FDS6982AS
H4
H7
1x9
R52 54.9K
R53 1.13K
R51 54.9K
R50 1.13K
BATTER2 HEADER
BATTER1 HEADER
Q19
Q20
Q17
Q18
R116 10E
CB64 1uF
Q14
NX7002AK_300mA/60V
D5
LED-S-G-081604
R5 330E
VLIM SELECT JUMPER
S_JPX1
86730-001LF
25-14001-1020
JPX1
2 Cell
3 Cell(*)
PH-1*3-2D54-D-ST-ML-6/3
21-6110E-1030
RX3 10K
VLIM=8.2V
VLIM=12.6V
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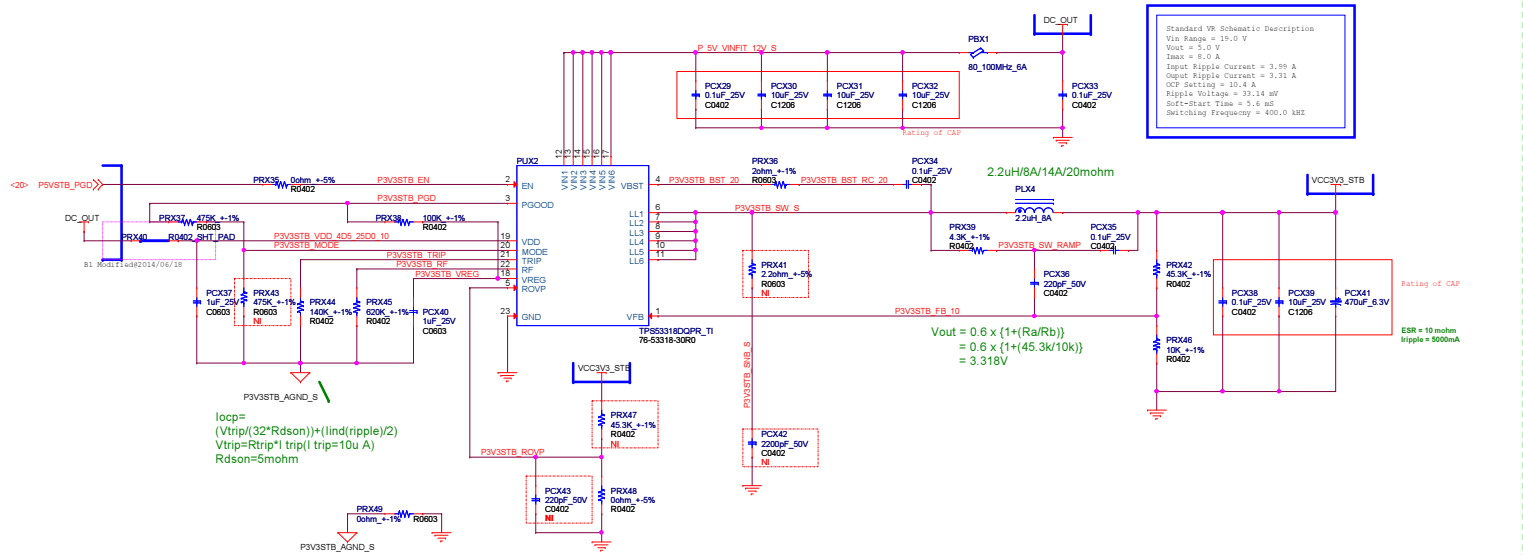
Title
9-16V INPUT POWER SUPPLY
Size A2
Document Number
MiniBase-10R
Rev B1
Date: Monday, July 21, 2014
Sheet 14 of 21

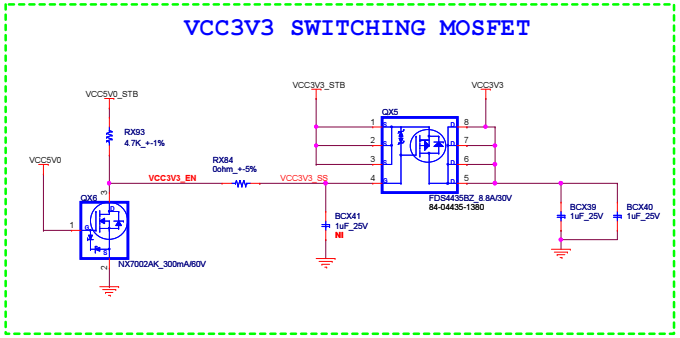
A2 Modify:
1. Change LTC3728 to LTC3789(VCC5V0_STB) and TPS53318(VCC3V3_STB)
2. Add PMOS to switch VCC3V3 when power up
3. Loaded R63 to solve Express-TCR boot fail problem
4. Change Q11 softstart to R/C to reduce inrush current when switching on
5. Add an offpage symbole from POWER_EN to QX1.4 for ATX mode

BOM remove:
1. U8(76-03728-52R0)
2. Q15,Q16,Q21,Q22(84-09003-0360)
3. D8,D9(83-R2003-0810)
4. L2(68-47210-1170)
5. L3(68-10310-1000)
6. TP27,TP28
7. Q9(84-07002-0310)
8. CB51,CB52,CB67,CB76,CB77(80-33612-1680)
9. CB66,CB92(78-22622-2240)
10. CB53,CB91(78-10622-2260)
11. C46(80-33713-6780)
12. CB78(78-47522-2640)
13. CB54,CB72,CB85,CB87,CB93(78-10524-2640)
14. C45,CB68,CB69,CB80,CB84(78-10421-2440)
15. CB70,CB71,CB79,CB83(78-10224-2460)
16. CB73,CB82(78-12124-2470)
17. R104,R133,R138(63-15303-4410)
18. R124,R125,R130(63-10303-4410)
19. R110(64-R0105-21D0)
20. R175(64-R0205-1610)
21. R128(64-10R05-4490)
22. R118(64-12115-4490)
23. R163(64-20015-4490)
24. R103,R129(64-49915-4420)
25. R169(64-63415-4490)
26. R112(64-64915-4410)
27. R97,R102,R121,R122,R132,R142,R143(63-R0003-4420)
28. R98(63-10203-4410)

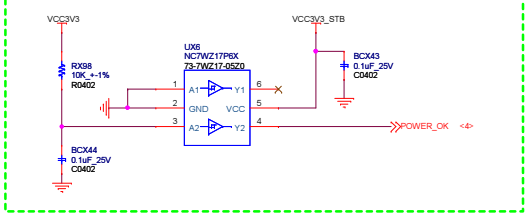
VCC3V3_STB POWER SUPPLY

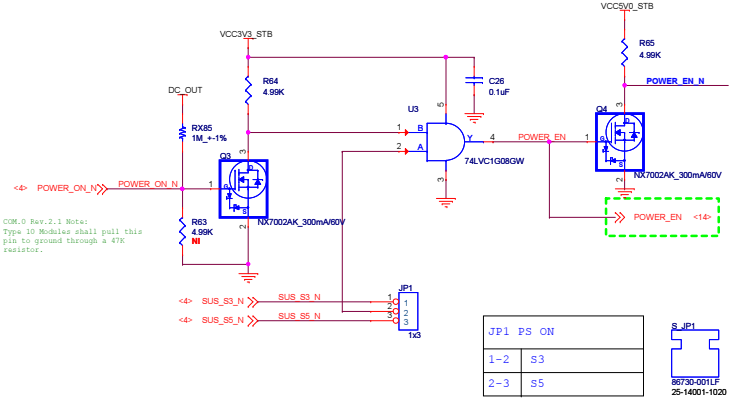


VCC3V3 SWITCHING MOSFET



Carrier Board Power OK

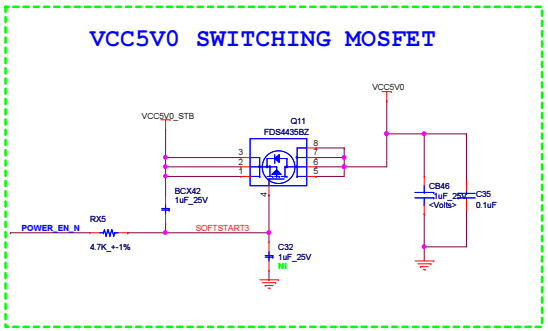


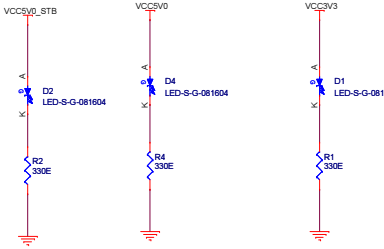


JP1	PS ON
1-2	S3
2-3	S5

S_JP1
86730-001LF
25-14001-1020

VCC5V0 SWITCHING MOSFET





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Title: 5V AND 3.3V POWER SUPPLY

Size	Document Number	Rev
A2	MiniBase-10R	B1

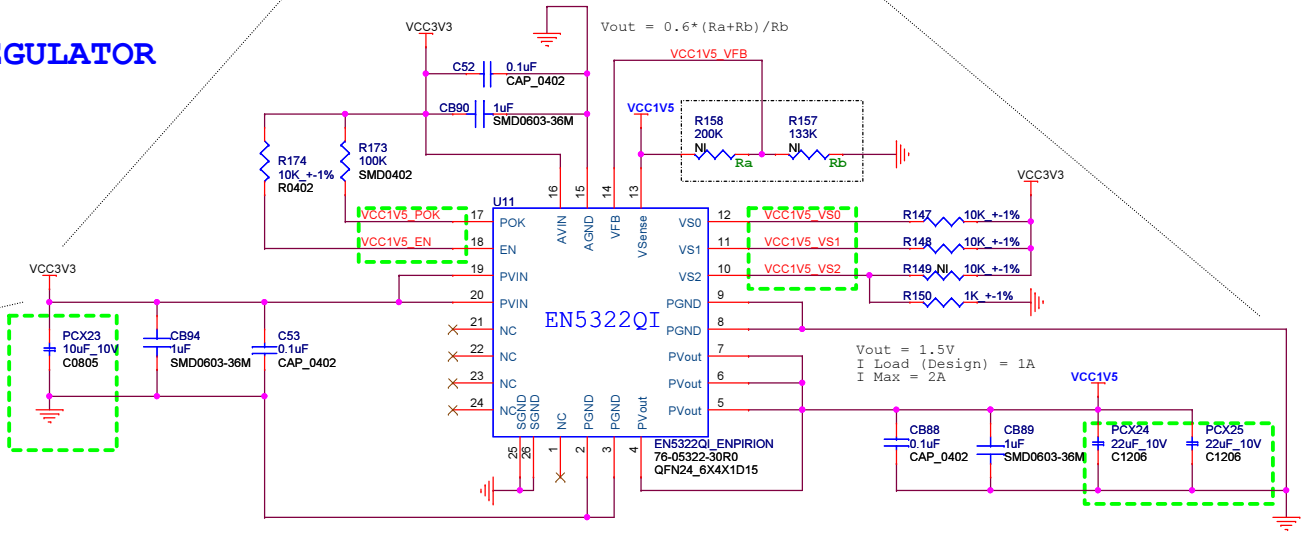
Date: Monday, July 21, 2014 Sheet 15 of 21

1.5V POWER SUPPLY

1.5V SWITCHING REGULATOR

Keep the input and output current loops separate from each other as much as possible. Keep sensitive signals away from the power supply circuit.

Keep the input circuit of any converter away from the output circuit of any other converter.



A2 Modify:
1. Remove VCC2V5 circuit sense SDVO to DVI has removed.(design change)
2. Used PUX2(TPS53318) power solution to instead of U13 power design.
3. U11 footprint and symbol (U11.4 need connect to Vout)
4. Replace CB95(C0603/X5R) to PCX23(C0805/X7R)
5. Replace CB81,CB86(C0805/X5R) to PCX88,PCX89(C1206/X7R)
6. Remove TP16 useless item.
5. Add net name for VS0-2,POK and EN.

BOM change:
1. Remove: U17,R215,C69,C72,CB105,CB107,CB108,CB118
2. Remove U13,C54,C55,CB96,CB97,CB98,CB99,CB100,CB101,CB102,TP17
3. Remove R176,R177,R182,R183,R186,R187,R188,R194,R195,R196

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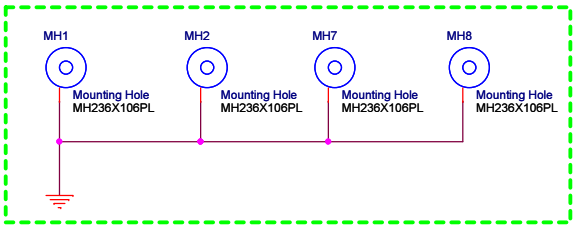
Title		
1.5V_STB POWER SUPPLY		
Size A3	Document Number MiniBase-10R	Rev B1
Date: Monday, July 21, 2014	Sheet 16 of 21	

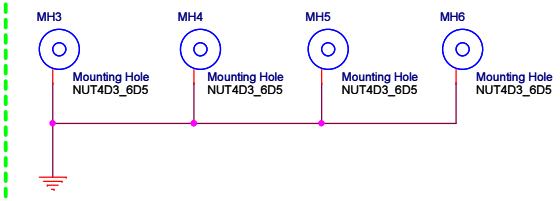
A2 Modify: (SCH)
1. Correct board mounting holes from MH2,MH3,MH7,MH8 to MH1,MH2,MH7,MH8

BOARD MOUNTING HOLES

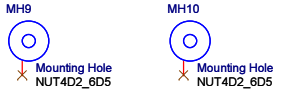


A2 Modify:
1. Correct board mounting holes from MH1,MH4,MH5,MH6 to MH3,MH4,MH5,MH6 (SCH)
2. Change module mounting holes size (sample as Express-Base, footprint change)
Standoff P/N: 33-72000-0080

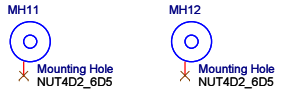
MODULE MOUNTING HOLES



MINI PCIE1 FIXED HOLES



MINI PCIE2 FIXED HOLES



A2 Modify:
1. Add MH9 and MH10 for J2 (co-layout)
2. Add MH11 and MH12 for J5 (co-layout)
Standoff P/N: 33-72013-1P50

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Title		
MECHANICAL		
Size: A3	Document Number: MiniBase-10R	Rev: B1
Date: Monday, July 21, 2014	Sheet 17 of 21	

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Title		
BLANK		
Size: A3	Document Number: MiniBase-10R	Rev: B1
Date: Monday, July 21, 2014	Sheet 18 of 21	

REVISION HISTORY

REVISION	DATE	CHANGES
A1	JAN-11-2012	Initial Release
A2	FEB-1-2013	1. Correct U9.13 from GND to CB_RESET_N to solve H6 workless issue P.04 Correct FAN_IN to Q8.3, DC_OUT_9-16V to Q8.2 to solve FAN speed issue Change R91 power source from DC_OUT_9-16V to DC_OUT_9-16V_M Correct H3 symbol pin define and footprint to solve FAN connector reverse issue Used the same pin wide lines to instead of the VCC5V0_STB and DC_OUT_9-16V_M power shapes (layout) Change J4 VCC power source from DC_OUT_9-16V to DC_OUT_9-16V_M Replace S1-S4 to general DIP component by purchase requirement (footprint change) Remove R159 and NET:LPC_CLK_DBG sense H6 has removed. BOM change: a. Replace S1-S4 from 62-49020-0000(SMT) to 22-48000-0010(DIP) b. Remove R159: 64-33R05-4490(33 ohm, R0402) 2. Add 2 jumper selection to switch AT/ATX P.04 P.14 Replace all jump size to pitch 2.54mm to solve production issue BOM change: a. Add JPX2,JPX3: 21-6110E-1030 S_JPX2,S_JPX3: 25-14001-1020 b. Replace S_JP1-S_JP7 from 25-10013-1020 to 25-14001-1020 3. Correct U15 and U16 to solve boot up failed problem P.05 Remove H6 sense it already has LPC-CPLD to decode message. BOM change: a. Replace U15 from 73-00102-00Z0 to 74-00102-08Z0 U16 from 73-00104-00Z0 to 73-00104-01Z0 b. Remove H6: 61-7540B-2050 4. Correct audio jack symbol and JDREF design to solve soundless problem P.06 BOM change: a. Replace J15(21-92001-0090) to JX1(20-92000-0090) J16(21-92041-0050) to JX2(20-92080-0050) R26 from 10K(64-10025-4490) to 5.1K(64-51015-4490) R25 from 1K(63-10203-4410) to 10K(64-10025-4410) b. Add RX1(64-20025-4420) for JDREF(U2.40) 5. Replace J12 and J14 to solve LAN LED working abnormal problem P.08 Change USB2/USB3 power source from VCC5V0 to VCC5V0_STB to solve system auto wake up issue when entering to S3 mode BOM change: a. Replace J12(21-F2010-0240) to JX4(21-F2020-0220) J14(21-92002-0140) to JX3(21-92000-0140) 6. Correct J7.11 from dummy to GND to solve detection problem (layout) P.10 Add mutil selection for U10 to support both 9DB403(0~70 degree) and 9DB433(-40~85 degree) BOM change: a. Replace R161 from 1K(63-10203-4410) to 10K for 9DB433 b. DNP R6,R140,R167,R170: 63-10303-4410(10K ohm, R0402) R135: 63-10203-4410(1K ohm, R0402) c. Add RX10,RX13: 63-R0003-4510(0 ohm, R0603) RX11,RX12: (10K ohm, R0402) 7. Change USB0/USB1/USB7 power source from VCC5V0 to VCC5V0_STB to solve system auto wake up issue when entering to S3 mode (layout) P.11 8. Correct ESD component from to to solve VCC_5V0 leakage when plug-in external DVI Video cable P.12 BOM change: a. Replace P6,P6,P8(69-91053-0000) to PX1,PX2,PX3(69-91026-0K10) 9. Correct BATT1 and BATT2 implementation to solve battery charging control issue. P.14 Change J1 to JX1 for standard. Add a PMOS control circuit to solve ATX mode control issue Add a discharger circuit to solve DC_OUt_9-16V_M discharge too long problem. Add JPX1 for VLIM selection Correct L1 value from 0.47uH to 10uH for 4A current limit requirement. BOM change: a. Replace L1 from 68-47110-1070 to 68-10310-13Q0 J11 from 61-H2R03-0190 to 61-H2R03-1900 J1(20-42001-0040) to JX5(20-92040-0030) R51,R52 from 64-54R95-1410(54.9E) to 64-54915-4410(54.9K) b. Add RX6: 64-10015-4510 (1K ohm, R0603) RX3,RX7: 64-10025-4410 (10K ohm, R0402) RX8: 64-47015-4490 (4.7K ohm, R0402) RX2,RX9: 64-10035-4420 (100K ohm, R0402) BCX1: 78-10524-2640 (1uF/50V, C0805) QX1: 84-04435-0380 (PMOS, Si4435DDY) QX2: 84-07002-0310 (NMOS, 2N7002) QX3: 84-00138-0310 (NMOS, BSS138LT1G) UX1: 73-07414-0D00 (single schmitt-trigger invertor gate, 74AHC1G14) JPX1: 21-6110E-2040 (2*4 pin header)

REVISION	DATE	CHANGES
A2	FEB-1-2013	10. Correct J11 from 61-H2R03-0190 to 61-H2R03-1900 to solve SMT problem P.13 Correct H8 symbol pin define and footprint to solve backlight control issue Change R216,R219,JP6.1 power source from DC_OUT_9-16V to DC_OUT_9-16V_M BOM change: a. Replace J11 from 61-H2R03-0190 to 61-H2R03-1900 11. Add a pull up resistor to VCC on SOFTSTART1 for discharge to solve cold-boot issue at AT mode P.15 Populate R63 to solve system boot-up/working abnormal issue Add R/C softstart on Q11 gate to reduce inrush current when VCC_5V0 switching on Add an offpage symbole from POWER_EN to QX1.4 for ATX mode Increase trace wide for Q21.3/Q15.3 to GND to solve four-corner failed issue (layout) Correct D8,D9 footprint from SMD-VMN2 to SDIO_SOD523_SC79 to solve solder issue BOM change: a. Add RX4: 64-10045-4490 (1M ohm, R0402) RX5: 64-47015-4490 (4.7K R0402) b. Replace C32 from 78-10421-2440(0.1uF) to 78-10521-0560(1uF) c. Delete R98: 63-10203-4410 (1K ohm, R0402, DNP) R104: 63-15303-4410 (15K ohm, R0402) 12. Correct board mounting holes from MH2,MH3,MH7,MH8 to MH1,MH2,MH7,MH8 (SCH) P.17 Correct board mounting holes from MH1,MH4,MH5,MH6 to MH3,MH4,MH5,MH6 (SCH) Change module mounting holes size thant same as Express-Base (footprint change) Add new fixed pad with H=1.5mm standoff(33-72013-1P50) for J2 and J5(co-layout) BOM change: a. Add J2-J5: 33-72013-1P50 (H=1.5mm standoff) b. Replace MH3-MH6 from MH236X106PL to NUT4D2_7 (footprint change) 13. Add PUX1 Buck-Boost power controller for FAN and LVDS backlight. P.04 P.13 BOM change: a. Add PUX1: 74-03789-08R0 PQX1,PQX2: 84-87350-03A0 PDX1: 83-R2003-0810 PDX2,PDX3: 83-1R004-02G0 PDX4,PDX5: 83-3R004-09M0 PLX2: 68-22210-11Q0 PLX1,PLX3: 68-10110-10Q0 PCX1: 78-10422-24A0 (0.1u/25v, C0402) PCX2,PCX3,PCX4: 78-10622-21B0(10u/25v, C1206) PCX5,PCX6: 78-10522-2540(1u/25v, C0603) PCX7: 78-10322-2400 (0.01u/50v, C0402) PCX8: 78-10224-2400 (1000p/50v, C0402) PCX9: 78-47322-24B0 (0.047u/25v, C0402) PCX10,PCX13: 78-22422-25B0 (0.22u/25v, C0402) PCX12: 78-10623-2640 (10u/10v, C0805) PCX14: 78-39134-14B0 (390p/50v, C0402) PCX15: 78-18224-24B0 (1800p/50v, C0402) PCX16,PCX21: 78-10421-2440 (0.1u/16v, C0402)) unfunished

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Title: REVISION HISTORY

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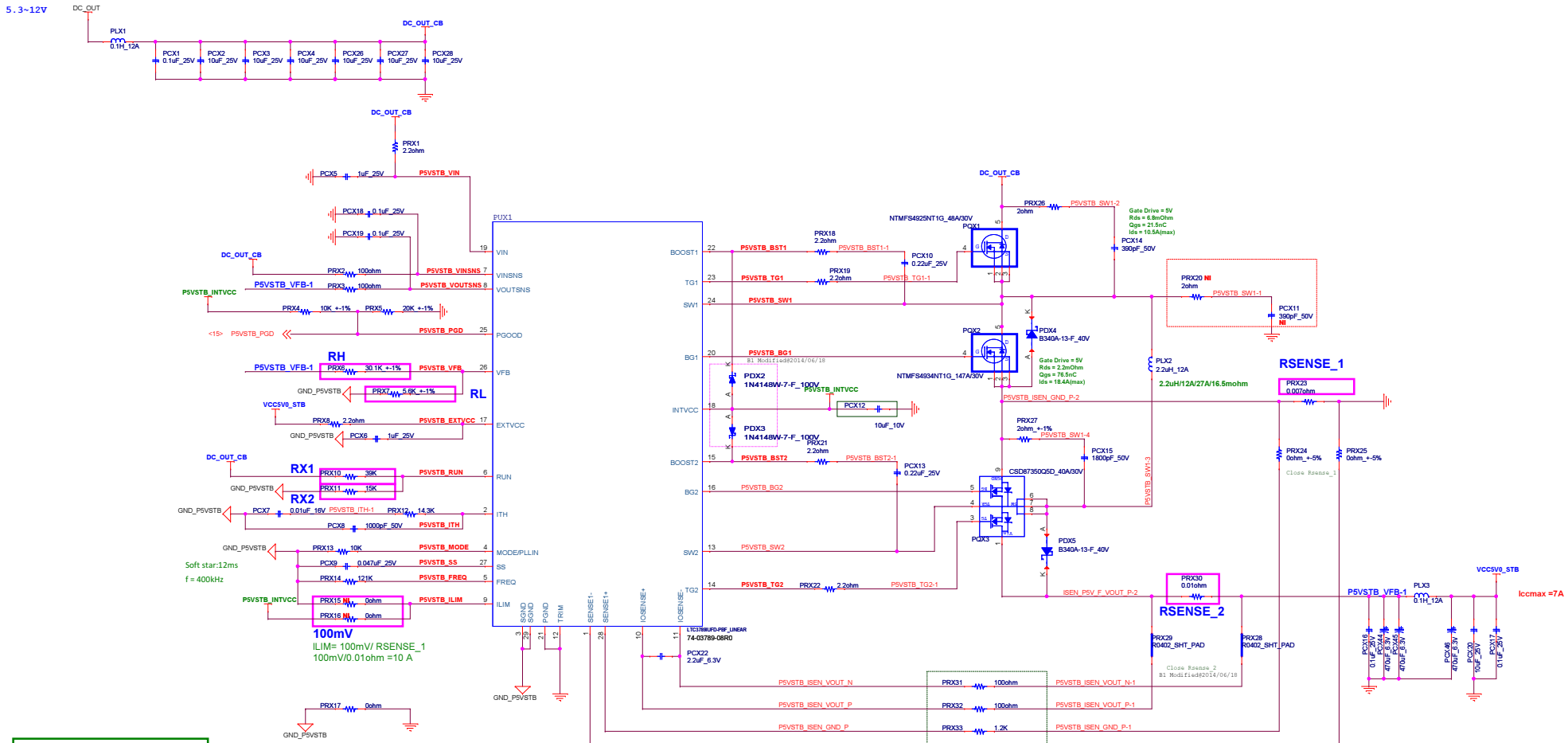

Vout= 0.8x(1+RH/RL)
0.8x(1+30.1/5.6)=5.1V

RUN, PGOOD Voltage .....6V to −0.3V
Vrun(on) = 1.22 V
Vdc-source = 5V to 20V
Vrun= Vdc-source x [RX2 / (RX1+RX2)]
20 x [15k / (15k+39K)) = 5.55V
5 x [15k / (15k+39K)) = 1.38V

Programming Input/Output Current Limit

The input/output current limit is set by the ILIM pin for 50mV, 100mV or 140mV with ILIM pulled to the GND, floating, or tied to INTVCC, respectively.

Fault Conditions: Current Limit and Current Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the boost region, maximum sense voltage and the sense resistance determine the maximum allowed inductor peak current, which is:

IL(MAX,BOOST) =140mV/RSENSE

In the buck region, maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current, which is:

IL(MAX,BUCK) =90mV/RSENSE

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Title	VCC5V0_STB_POWER_SUPPLY	
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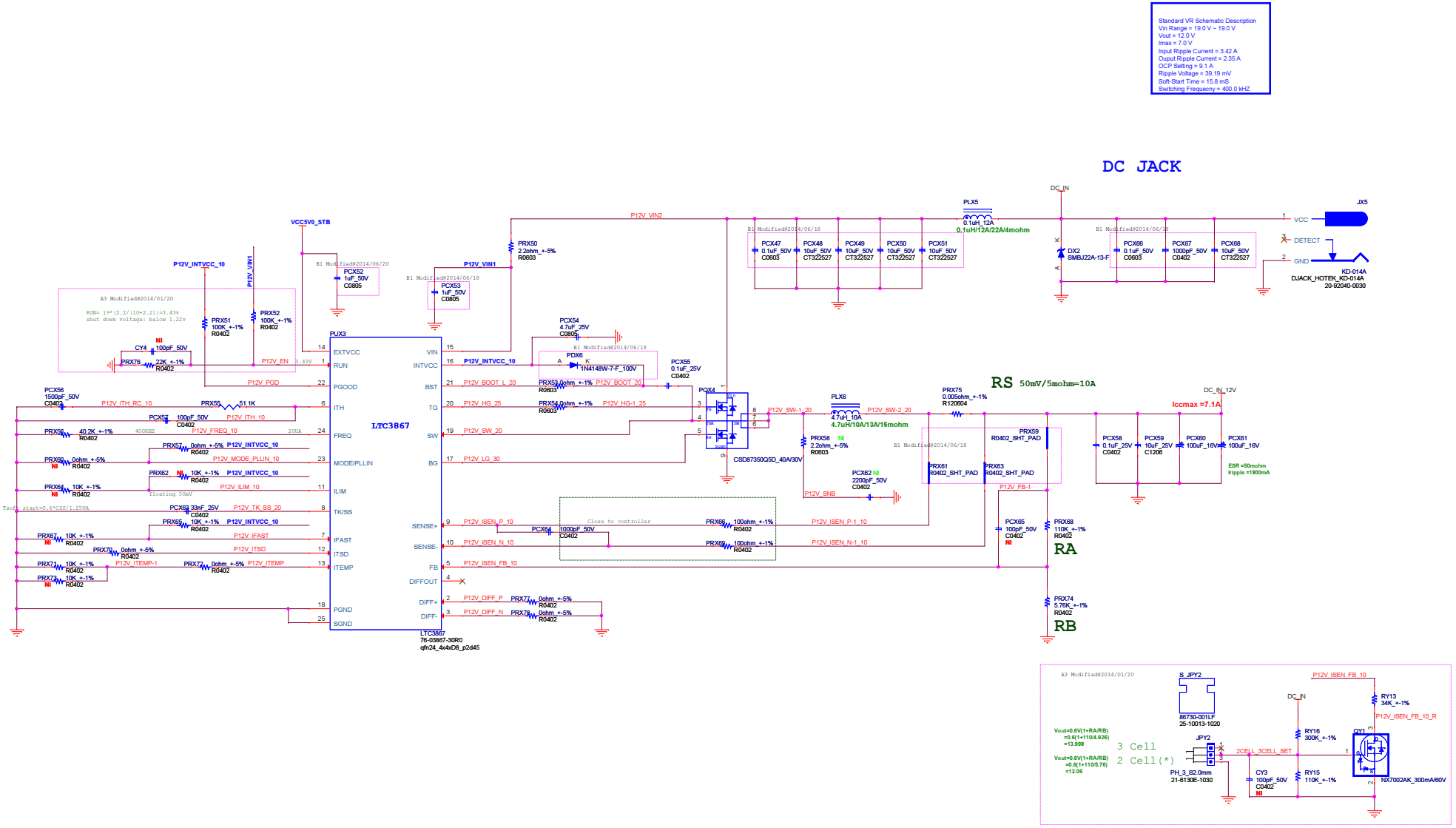
Standard VR Schematic Description
Vin Range = 18.0 V ~ 19.0 V
Vout = 12.0 V
Imax = 7.0 V
Input Ripple Current = 3.42 A
Ouput Ripple Current = 2.35 A
OCP Setting = 9.1 A
Ripple Voltage = 39.19 mV
Soft-Start Time = 15.8 mS
Switching Frequency = 400.0 kHZ
DC JACK
DC_IN
JX5
VCC
DETECT
GND
KD-014A
DJACK_HOTEK_KD-014A
20-62040-0030
PLX5
0.1uH_12A
0.1uH/12A/22A/4mohm
DX2
SMBJ22A-13-F
P12V_VIN2
VCCSV0_STB
P12V_INTVCC_10
P12V_VIN1
PUX3
LTC3867
EXTVCC
RUN
PGOOD
ITH
FREQ
MODE/PLLIN
ILIM
TK/SS
IFAST
ITSD
ITEMP
PGND
SGND
VIN
INTVCC
BST
TG
SW
BG
SENSE+
SENSE-
FB
DIFFOUT
DIFF+
DIFF-
LTC3867
76-03867-30R0
qfn24_4x4xD8_p2d45
RS 50mV/5mohm=10A
RA
RB
CSD87350Q5D_40A/30V
4.7uH_10A
4.7uH/10A/13A/15mohm
DC_IN_12V
Iccmax =7.1A
ESR =50mohm
Ripple =1800mA
S_JPY2
86730-001LF
25-10013-1020
JPY2
PH_3_S2.0mm
21-6130E-1030
3 Cell
2 Cell(*)
2CELL_3CELL_SET
NX7002AK_300mA/60V
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Title
DC_IN_12V_POWER_SUPPLY
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